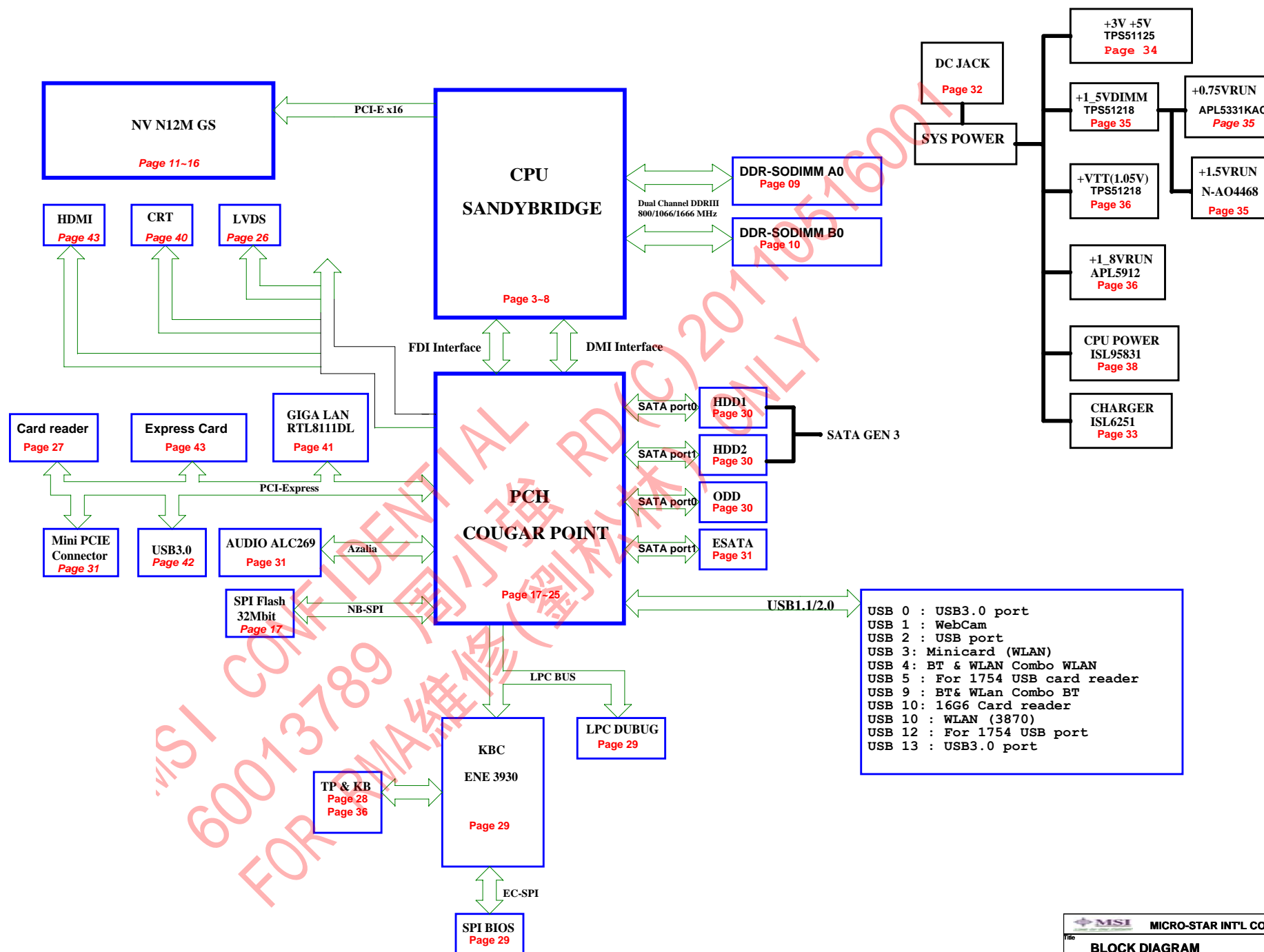


# Huron River Platform



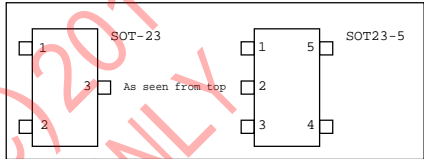
SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails			
POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	12V	S0, (S3-S5)	
+5VALW	5V	S0, (S3-S5)	
+5VRUN	5V	S0, S3	
+5VSUS	5V	S0	
+3VALW	3.3V	S0, (S3-S5)	
+3VRUN_CK505	3.3V	S0	Clock, MCH
+3VSUS	3.3V	S0, S3	
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0, (S3-S4)	DDR core
+1_5VSUS	1.5V	S0	
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDR command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC_GFXCORE	1.1V	S0	GMCH Graphics core rail

Net Naming Conventions

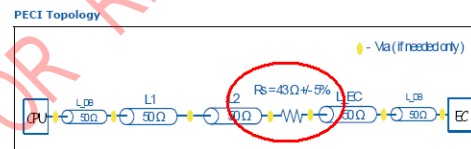
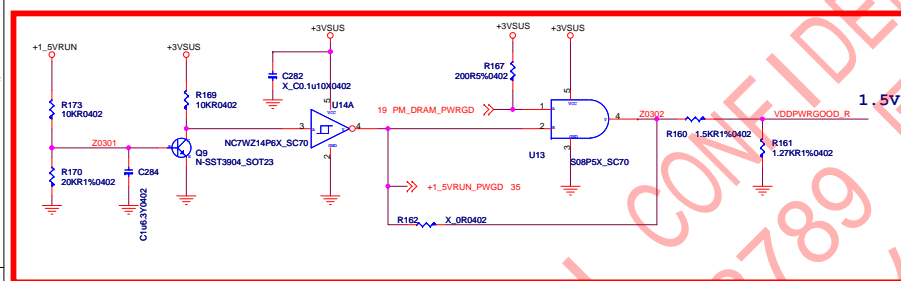
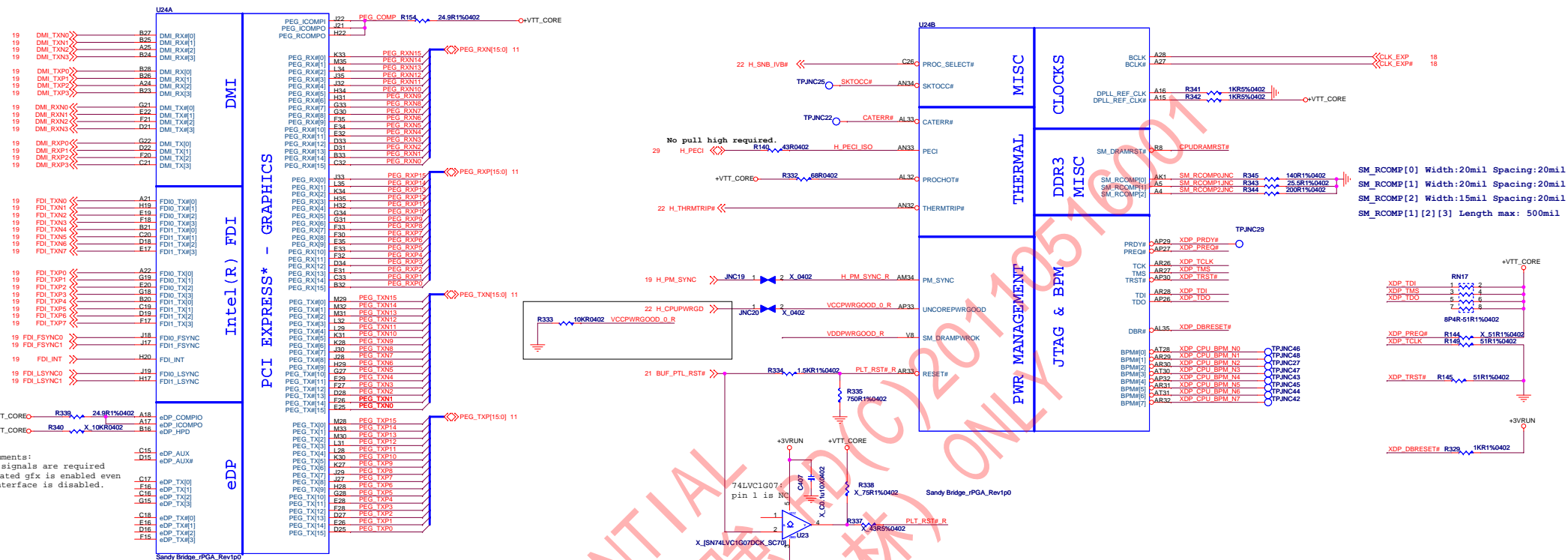
Suffix
# = Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



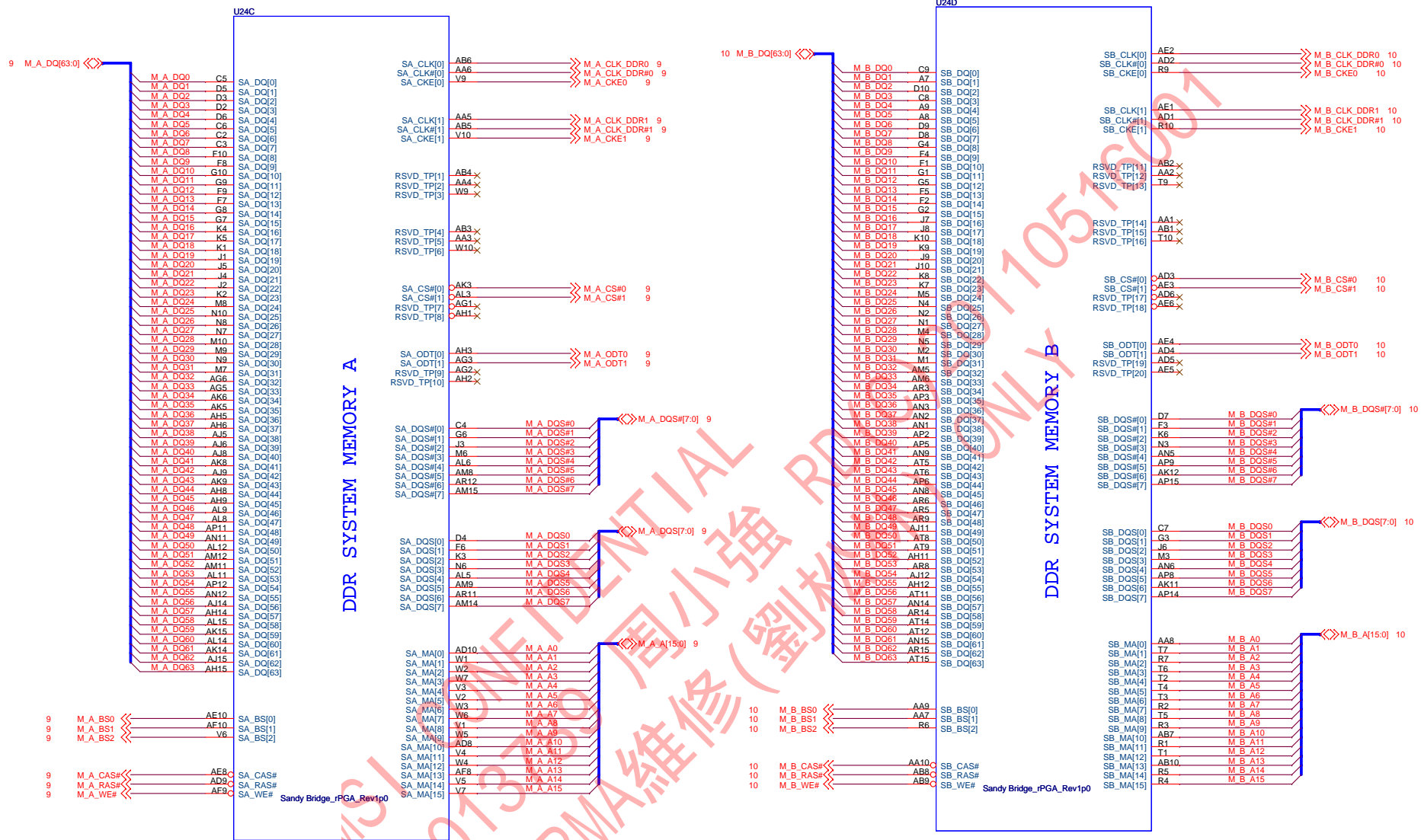
Power States	SLP S3#	SLP S4#	SLP S5#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	ON	OFF	OFF	OFF

**SANDYBRIDGE PROCESSOR (CLK,MISC,JTAG)**

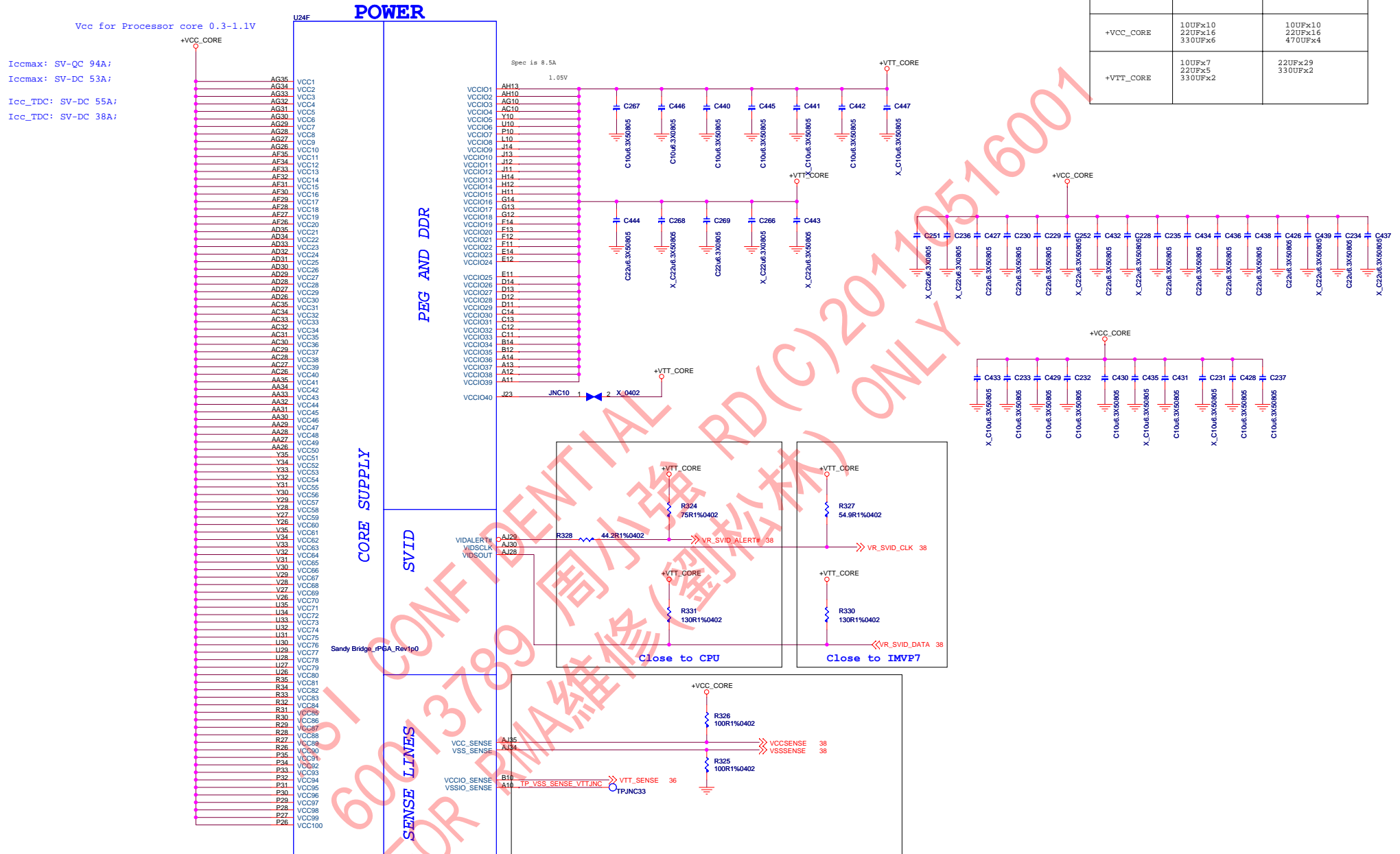


Title				
<b>PROCESSOR</b>				
Size	Document Number			Rev
Custom	<b>MS-16G9/1754</b>			0
Date:	Tuesday, September 14, 2010	Sheet	3 of 52	

## SANDYBRIDGE PROCESSOR (DDR3)

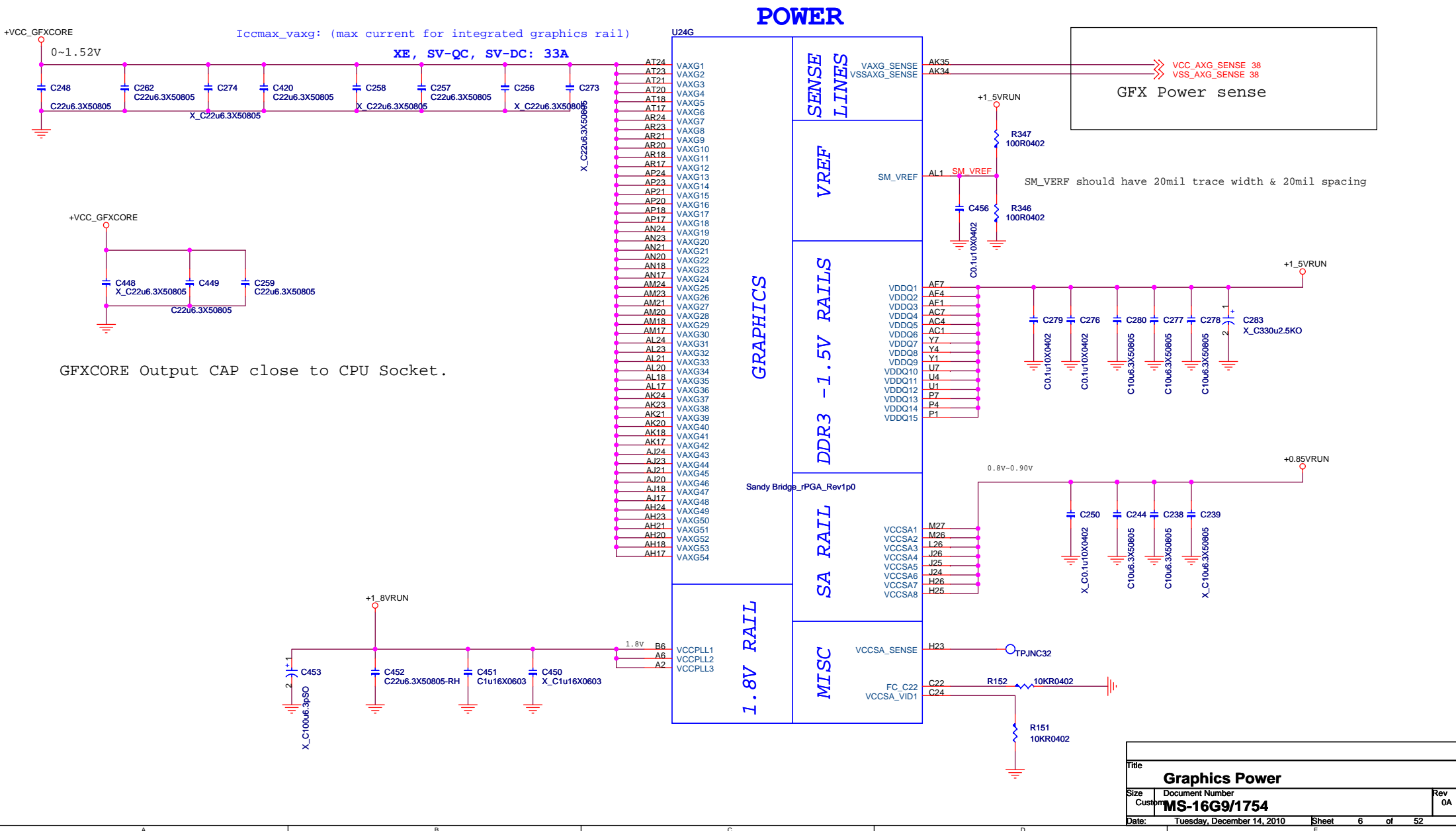


## SANDYBRIDGE PROCESSOR (POWER)

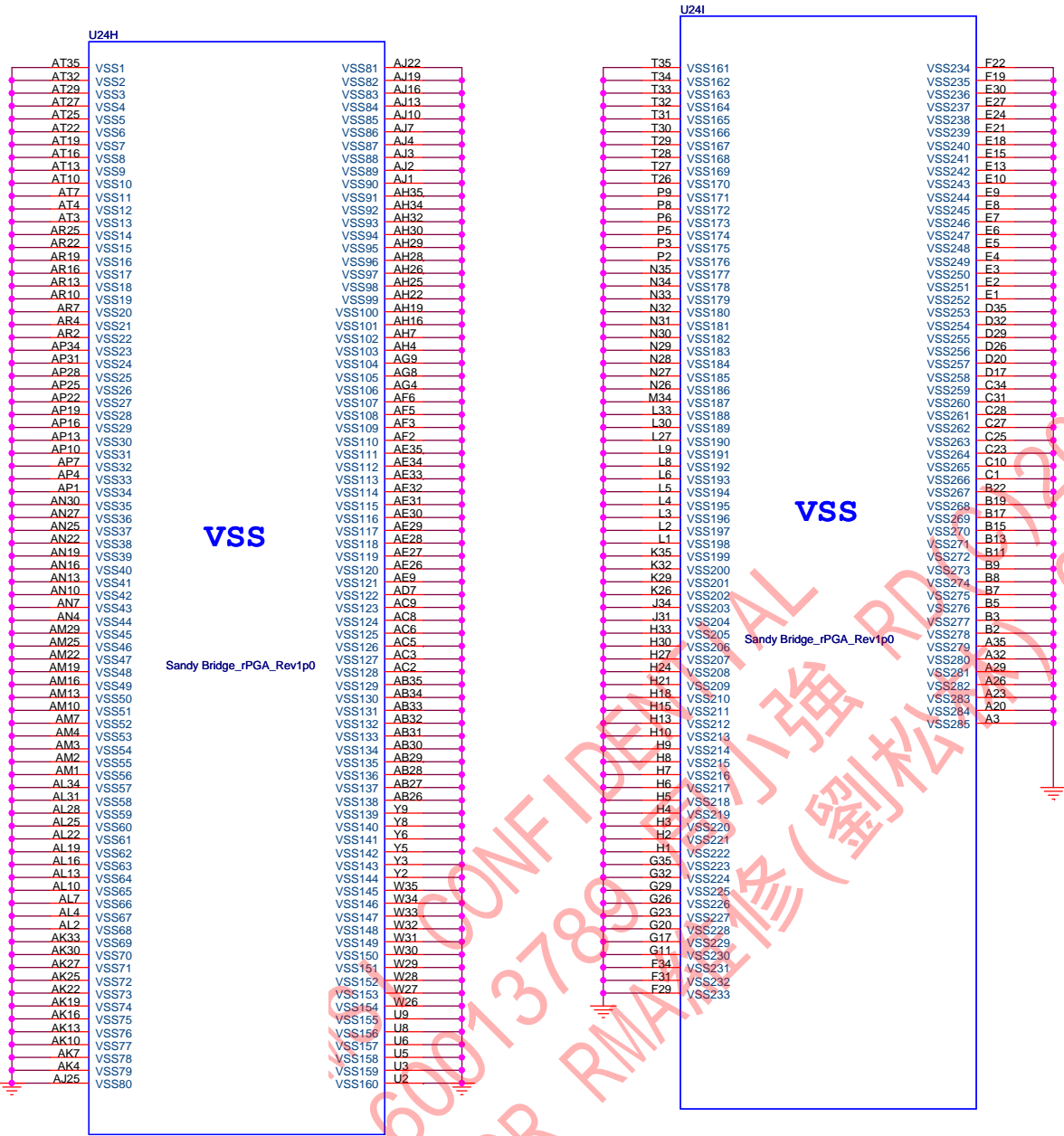


	148X schematic	CRB
+VCC_CORE	10UFx10 220UFx16 330UFx6	10UFx10 220UFx16 470UFx4
+VTT_CORE	10UFx7 220UFx5 330UFx2	22UFx29 330UFx2

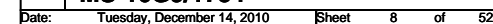
# SANDYBRIDGE PROCESSOR (GRAPHICS POWER)



SANDYBRIDGE PROCESSOR (GND)

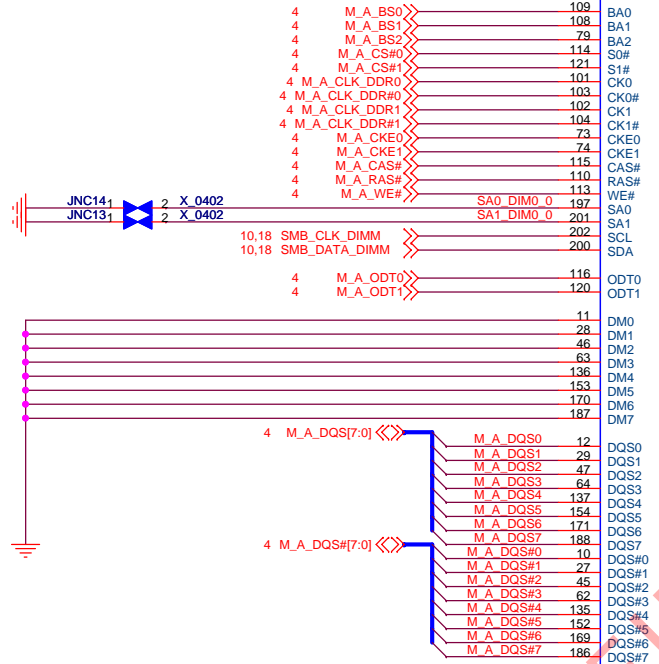


The CFG signals have a default value of "1" if not terminated on the board.

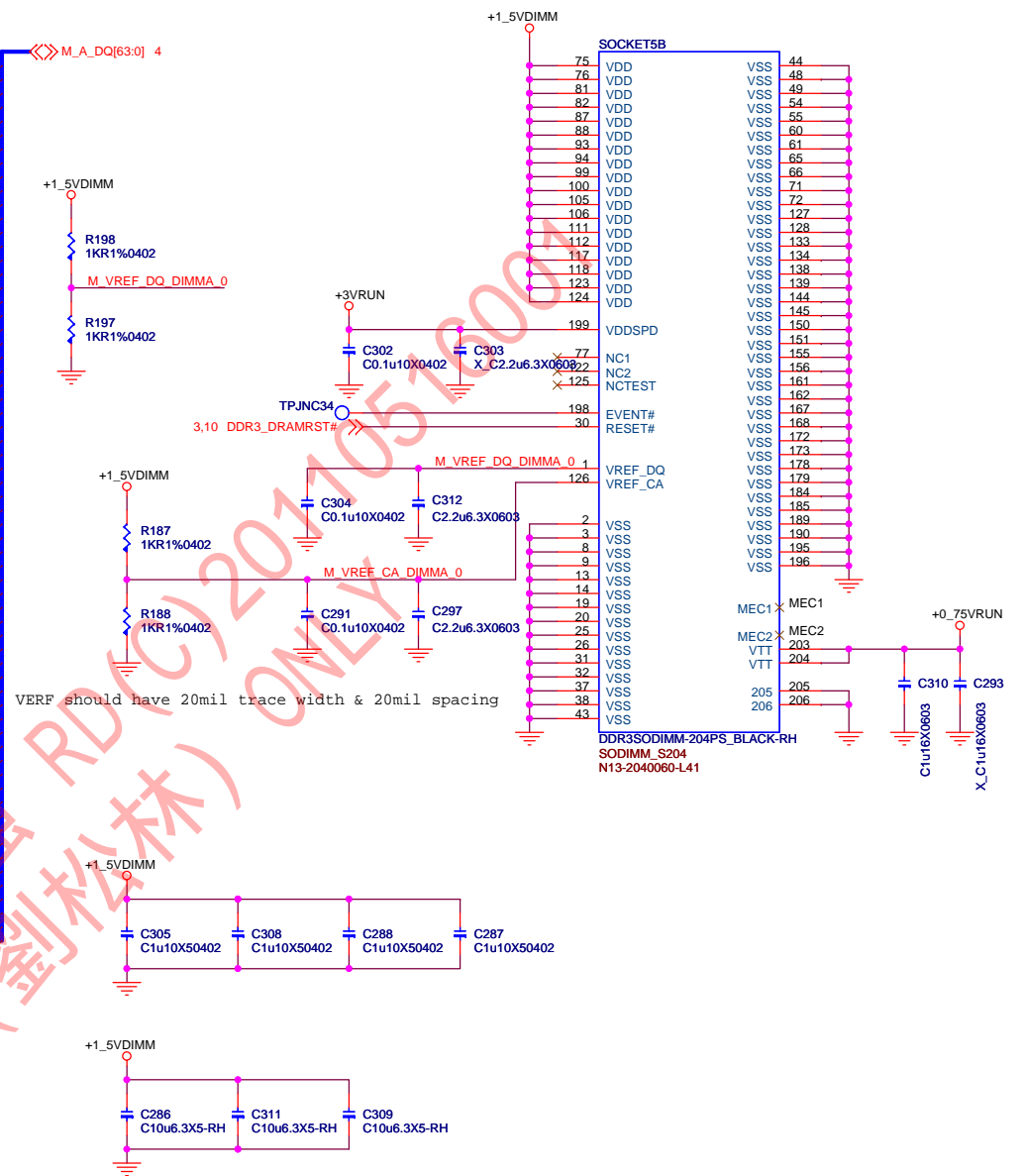




# SODIMM #A0

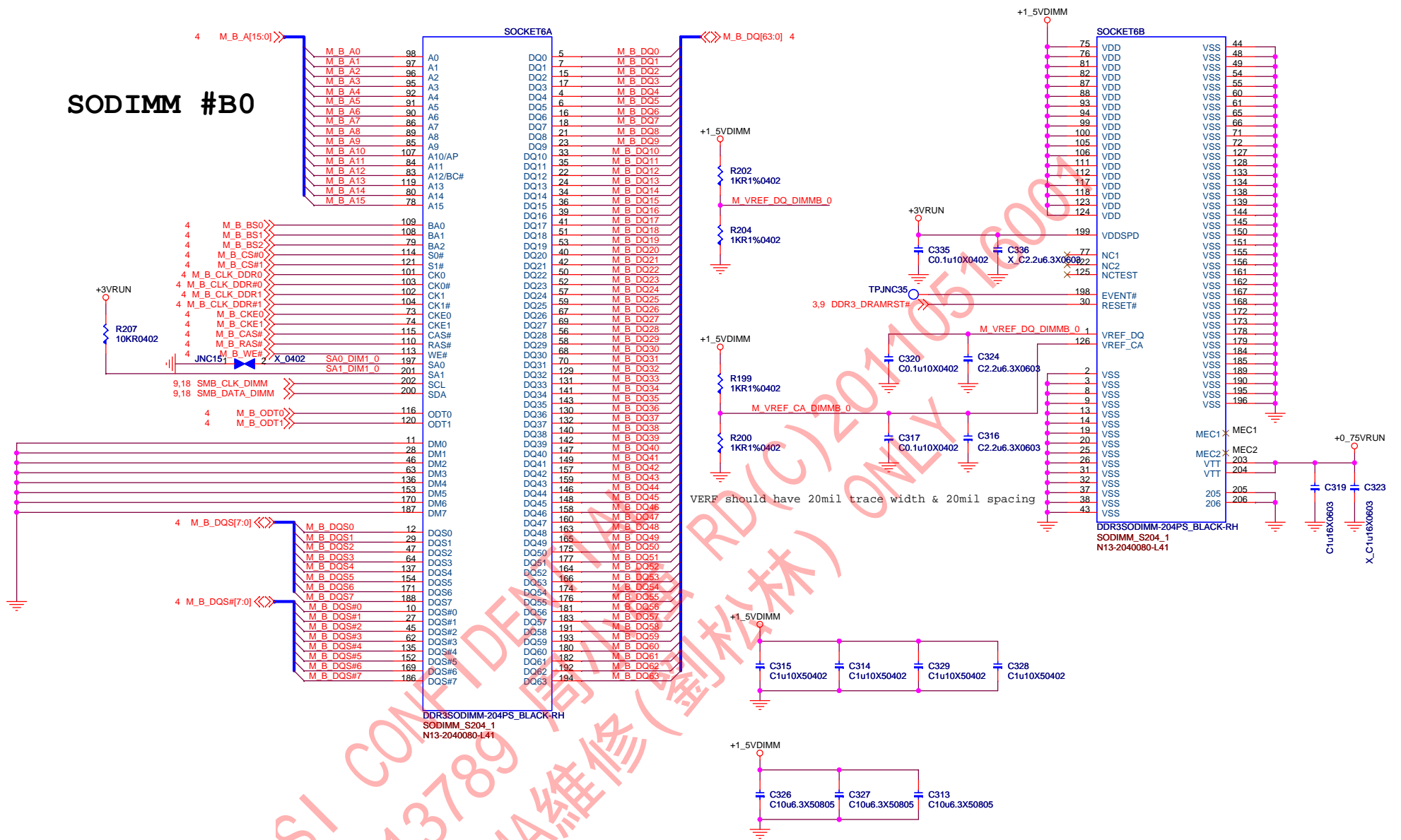


DDR3SODIMM-204PS\_BLACK-RH  
SODIMM\_S204  
N13-2040060-L41

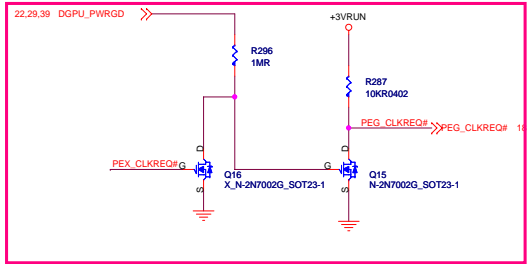


Title			Rev	
DDR3 SODIMM A0			0A	
Size	Document Number			
Custom	MS-16G9/1754			
Date:	Tuesday, December 14, 2010	Sheet	9	of 52

# SODIMM #B0



Title		
DDR3 SODIMM B0		
Size	Document Number	Rev
Custom	MS-16G9/1754	0A
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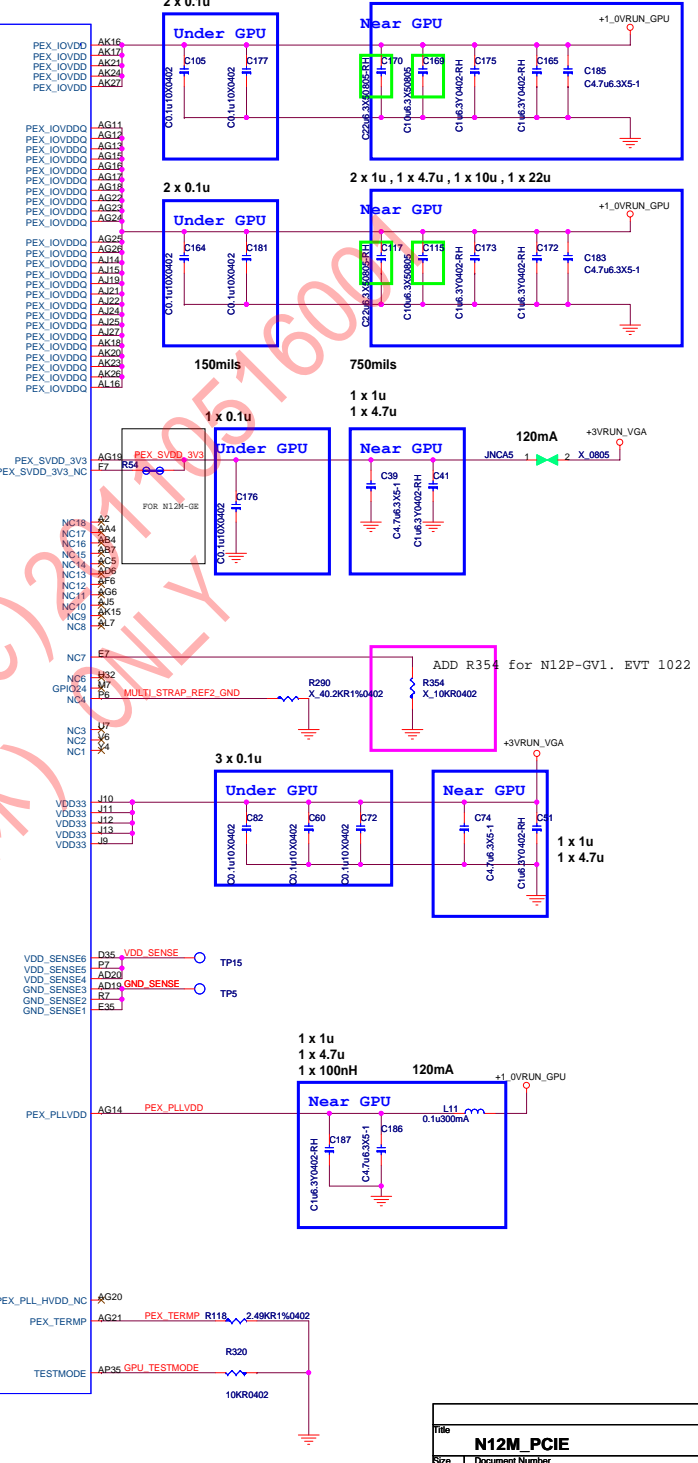
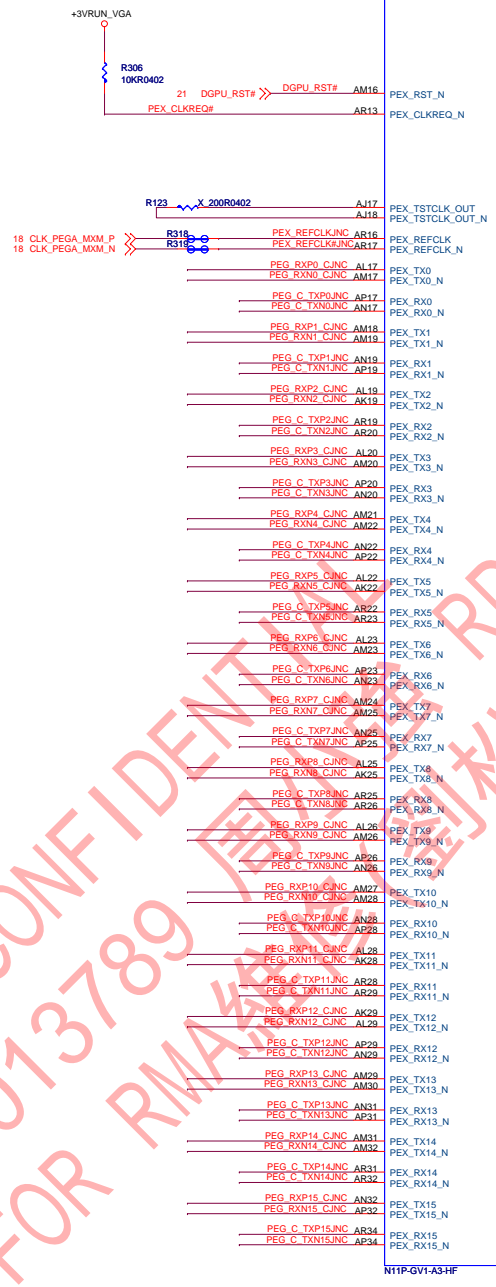
PEG\_RXN[15:0] << PEG\_RXN[15:0] 3  
PEG\_RXP[15:0] << PEG\_RXP[15:0] 3  
PEG\_TXP[15:0] << PEG\_TXP[15:0] 3  
PEG\_TXN[15:0] << PEG\_TXN[15:0] 3

PEG\_TXN0 C0.1u10X0402 C424 PEG\_C\_TXN0JNC  
PEG\_TXN1 C0.1u10X0402 C422 PEG\_C\_TXN1JNC  
PEG\_TXN2 C0.1u10X0402 C419 PEG\_C\_TXN2JNC  
PEG\_TXN3 C0.1u10X0402 C417 PEG\_C\_TXN3JNC  
PEG\_TXN4 C0.1u10X0402 C411 PEG\_C\_TXN4JNC  
PEG\_TXN5 C0.1u10X0402 C408 PEG\_C\_TXN5JNC  
PEG\_TXN6 C0.1u10X0402 C403 PEG\_C\_TXN6JNC  
PEG\_TXN7 C0.1u10X0402 C401 PEG\_C\_TXN7JNC  
PEG\_TXN8 C0.1u10X0402 C399 PEG\_C\_TXN8JNC  
PEG\_TXN9 C0.1u10X0402 C387 PEG\_C\_TXN9JNC  
PEG\_TXN10 C0.1u10X0402 C389 PEG\_C\_TXN10JNC  
PEG\_TXN11 C0.1u10X0402 C381 PEG\_C\_TXN11JNC  
PEG\_TXN12 C0.1u10X0402 C381 PEG\_C\_TXN12JNC  
PEG\_TXN13 C0.1u10X0402 C383 PEG\_C\_TXN13JNC  
PEG\_TXN14 C0.1u10X0402 C386 PEG\_C\_TXN14JNC  
PEG\_TXN15 C0.1u10X0402 C385 PEG\_C\_TXN15JNC

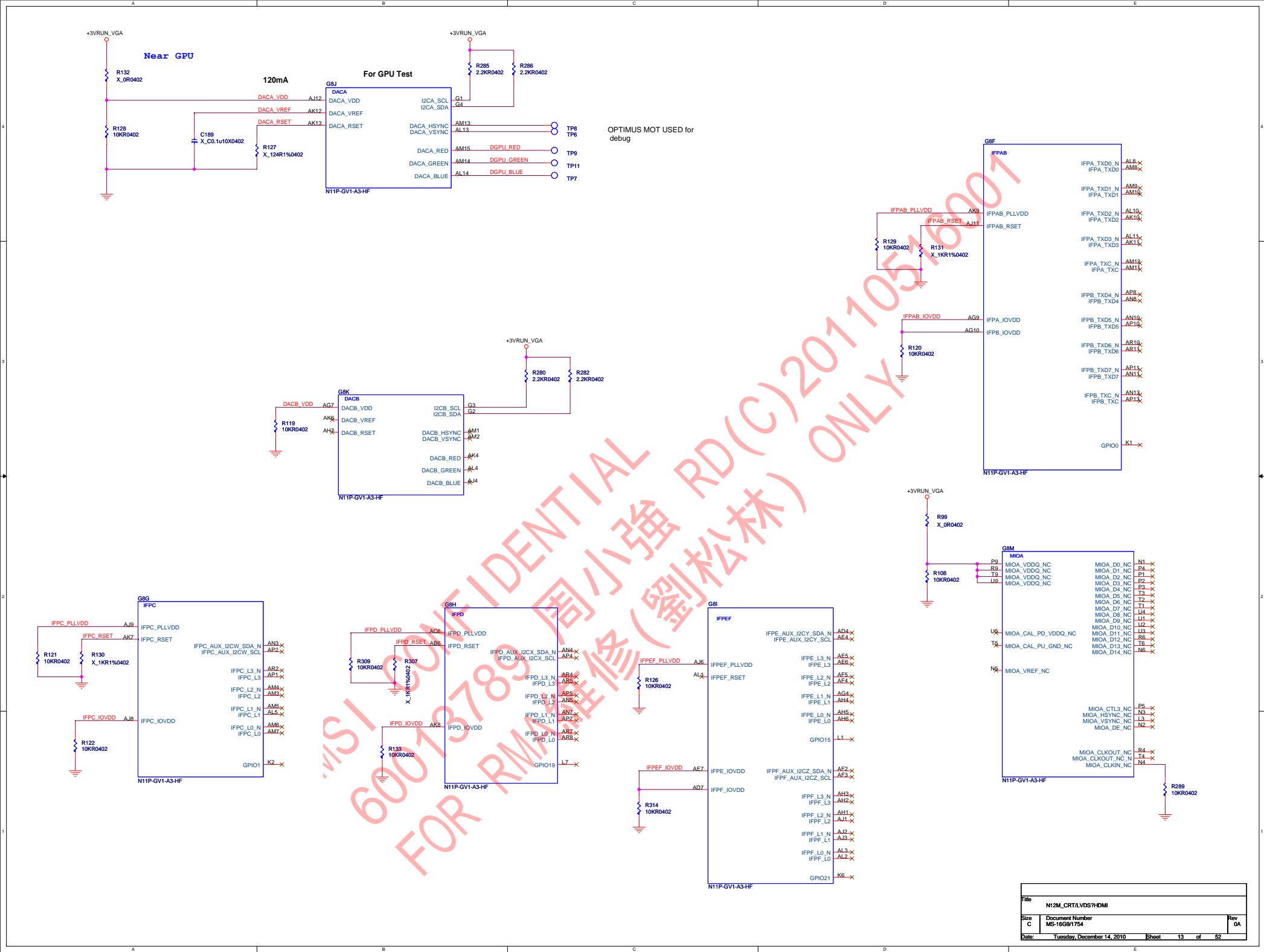
PEG\_TXP0 C0.1u10X0402 C425 PEG\_C\_TXP0JNC  
PEG\_TXP1 C0.1u10X0402 C423 PEG\_C\_TXP1JNC  
PEG\_TXP2 C0.1u10X0402 C421 PEG\_C\_TXP2JNC  
PEG\_TXP3 C0.1u10X0402 C418 PEG\_C\_TXP3JNC  
PEG\_TXP4 C0.1u10X0402 C416 PEG\_C\_TXP4JNC  
PEG\_TXP5 C0.1u10X0402 C410 PEG\_C\_TXP5JNC  
PEG\_TXP6 C0.1u10X0402 C404 PEG\_C\_TXP6JNC  
PEG\_TXP7 C0.1u10X0402 C402 PEG\_C\_TXP7JNC  
PEG\_TXP8 C0.1u10X0402 C400 PEG\_C\_TXP8JNC  
PEG\_TXP9 C0.1u10X0402 C398 PEG\_C\_TXP9JNC  
PEG\_TXP10 C0.1u10X0402 C396 PEG\_C\_TXP10JNC  
PEG\_TXP11 C0.1u10X0402 C388 PEG\_C\_TXP11JNC  
PEG\_TXP12 C0.1u10X0402 C380 PEG\_C\_TXP12JNC  
PEG\_TXP13 C0.1u10X0402 C382 PEG\_C\_TXP13JNC  
PEG\_TXP14 C0.1u10X0402 C385 PEG\_C\_TXP14JNC  
PEG\_TXP15 C0.1u10X0402 C394 PEG\_C\_TXP15JNC

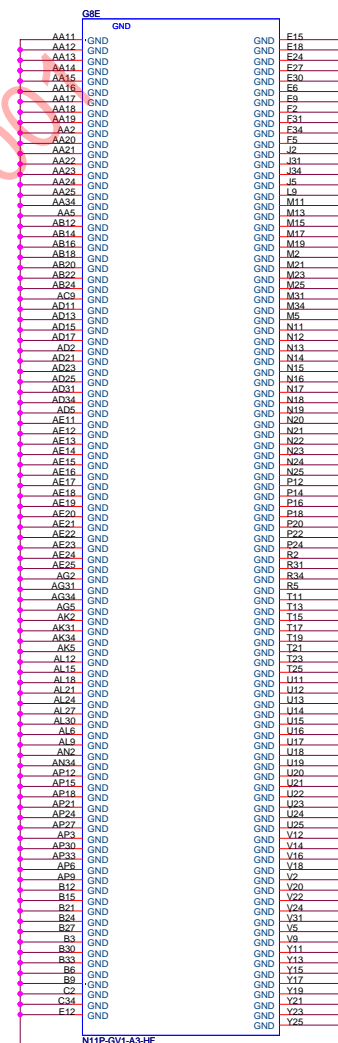
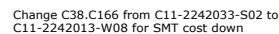
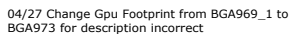
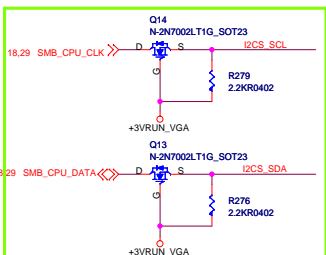
PEG\_RXN0 C202 C0.1u10X0402 PEG\_RXN0\_CJNC  
PEG\_RXN1 C210 C0.1u10X0402 PEG\_RXN1\_CJNC  
PEG\_RXN2 C198 C0.1u10X0402 PEG\_RXN2\_CJNC  
PEG\_RXN3 C211 C0.1u10X0402 PEG\_RXN3\_CJNC  
PEG\_RXN4 C195 C0.1u10X0402 PEG\_RXN4\_CJNC  
PEG\_RXN5 C209 C0.1u10X0402 PEG\_RXN5\_CJNC  
PEG\_RXN6 C191 C0.1u10X0402 PEG\_RXN6\_CJNC  
PEG\_RXN7 C205 C0.1u10X0402 PEG\_RXN7\_CJNC  
PEG\_RXN8 C194 C0.1u10X0402 PEG\_RXN8\_CJNC  
PEG\_RXN9 C219 C0.1u10X0402 PEG\_RXN9\_CJNC  
PEG\_RXN10 C207 C0.1u10X0402 PEG\_RXN10\_CJNC  
PEG\_RXN11 C223 C0.1u10X0402 PEG\_RXN11\_CJNC  
PEG\_RXN12 C215 C0.1u10X0402 PEG\_RXN12\_CJNC  
PEG\_RXN13 C221 C0.1u10X0402 PEG\_RXN13\_CJNC  
PEG\_RXN14 C214 C0.1u10X0402 PEG\_RXN14\_CJNC  
PEG\_RXN15 C226 C0.1u10X0402 PEG\_RXN15\_CJNC

PEG\_RXP0 C200 C0.1u10X0402 PEG\_RXP0\_CJNC  
PEG\_RXP1 C201 C0.1u10X0402 PEG\_RXP1\_CJNC  
PEG\_RXP2 C197 C0.1u10X0402 PEG\_RXP2\_CJNC  
PEG\_RXP3 C212 C0.1u10X0402 PEG\_RXP3\_CJNC  
PEG\_RXP4 C196 C0.1u10X0402 PEG\_RXP4\_CJNC  
PEG\_RXP5 C208 C0.1u10X0402 PEG\_RXP5\_CJNC  
PEG\_RXP6 C192 C0.1u10X0402 PEG\_RXP6\_CJNC  
PEG\_RXP7 C206 C0.1u10X0402 PEG\_RXP7\_CJNC  
PEG\_RXP8 C193 C0.1u10X0402 PEG\_RXP8\_CJNC  
PEG\_RXP9 C220 C0.1u10X0402 PEG\_RXP9\_CJNC  
PEG\_RXP10 C204 C0.1u10X0402 PEG\_RXP10\_CJNC  
PEG\_RXP11 C224 C0.1u10X0402 PEG\_RXP11\_CJNC  
PEG\_RXP12 C216 C0.1u10X0402 PEG\_RXP12\_CJNC  
PEG\_RXP13 C222 C0.1u10X0402 PEG\_RXP13\_CJNC  
PEG\_RXP14 C213 C0.1u10X0402 PEG\_RXP14\_CJNC  
PEG\_RXP15 C225 C0.1u10X0402 PEG\_RXP15\_CJNC



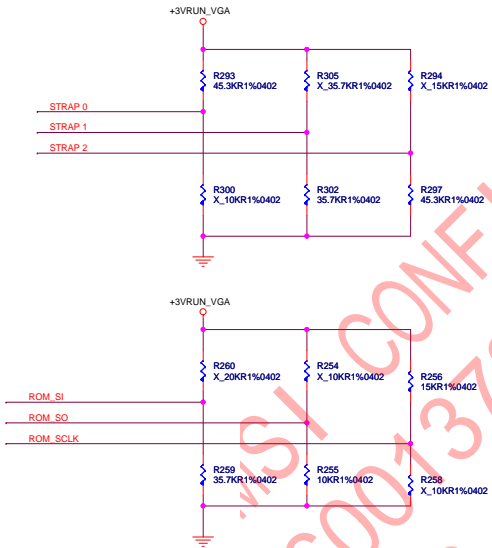
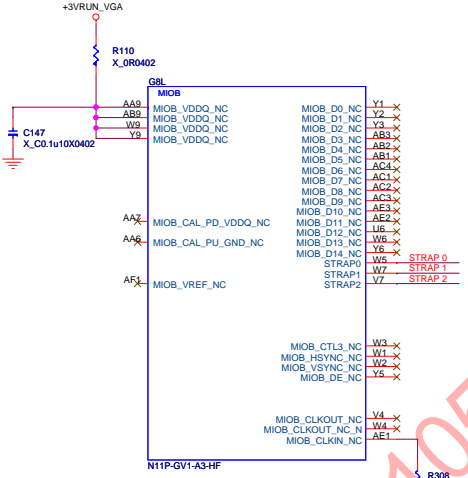
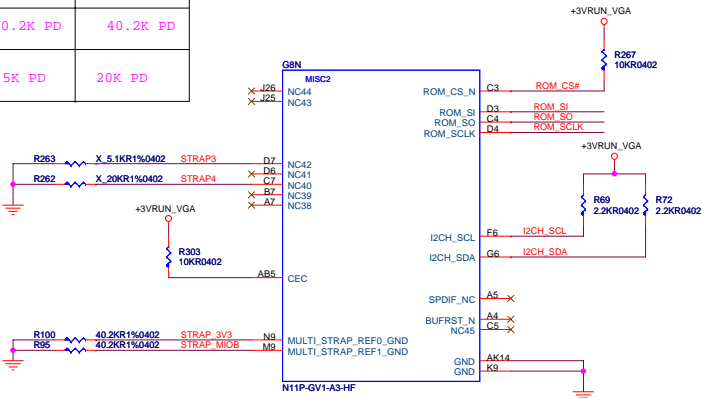






04/27 Change Gpu Footprint from BGA969\_1 to BGA973 for description incorrect

	Strap3	Strap4
N12M-GS1	40.2K PD	40.2K PD
N12P-GV1/GV	5K PD	20K PD

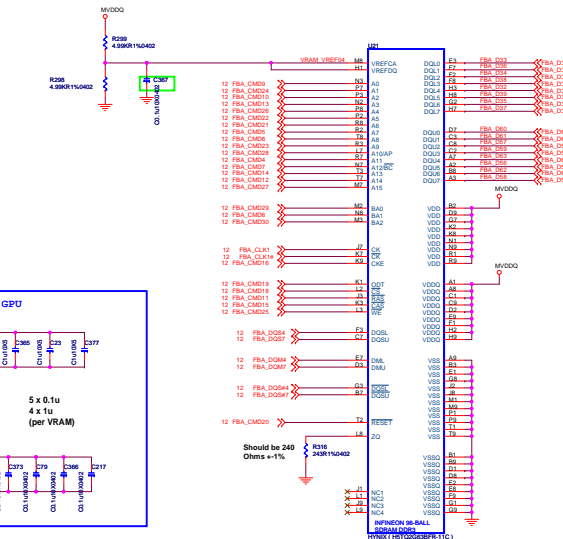
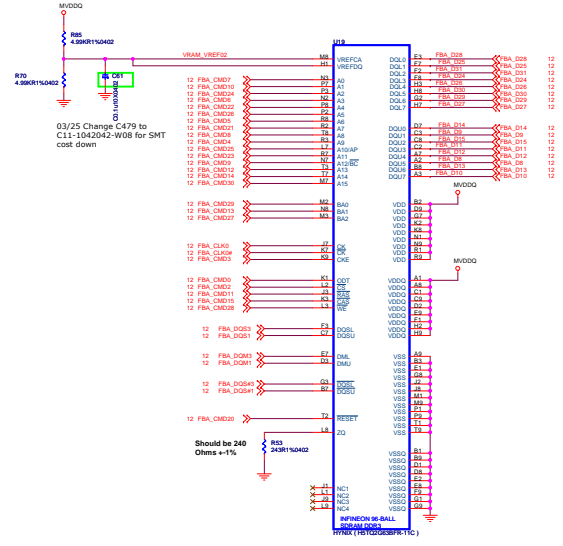
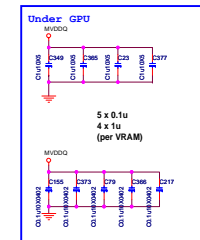
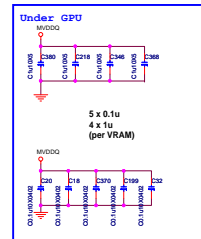
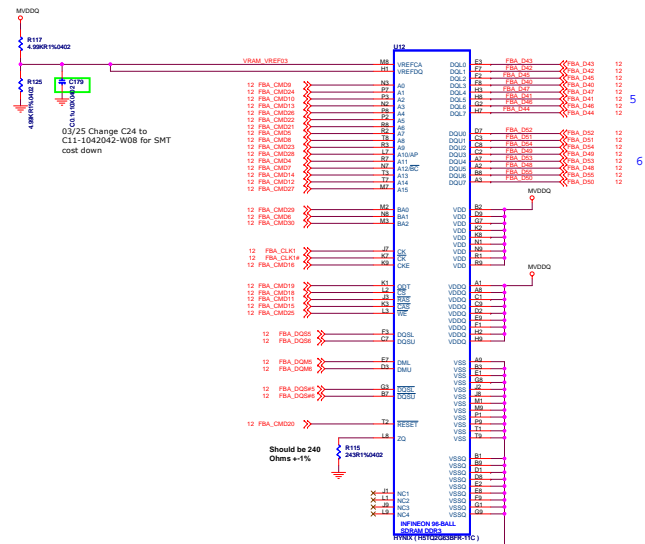
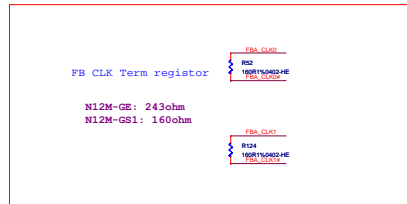
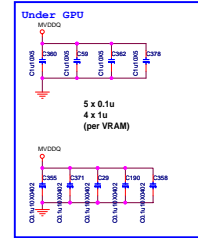
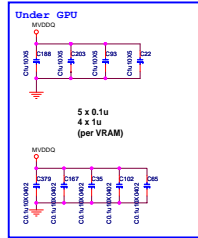
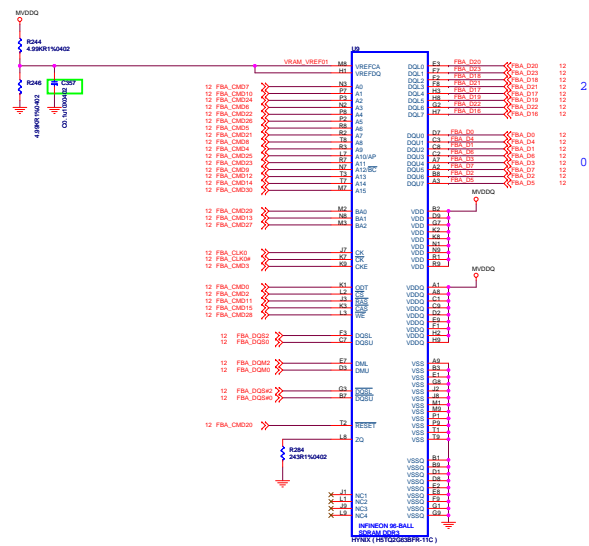


N12M		
STRAP0	USER 1	1
STRAP0	USER 2	1
STRAP0	USER 1	1
STRAP0	USER 0	1
STRAP1	USER 1	1
STRAP1	USER 0	1
STRAP2	USER 1	1
STRAP2	USER 0	1
ROM_SCLK	USER 1	1
ROM_SCLK	USER 0	1
ROM_SI	USER 1	1
ROM_SI	USER 0	1
ROM_SO	USER 1	1
ROM_SO	USER 0	1
VGA_DEVICE	USER 1	1
VGA_DEVICE	USER 0	1

STRAP0	PU 45K	SM BUS define resolution 1111
STRAP1	PU 15K	N12M-GS:PD 35K, N12M-GE:PU 35K N12M-GS1:PD 35K N12P-GV1: PD35K
STRAP2	PU 15K	N12M-GS:PD 25K, N12M-GE:PU 15K N12M-GS1: PU15K N12P-GV1: PD45K
ROM_SCLK	PU 15K	N12M-GS:PU 15K, N12M-GE:PU 15K, N12M-GS1:PD 15K
ROM_SI	PU 35K	Hynix 128Mx16----- PD35K Samsung 128Mx16----- PD45K
ROM_SO	PU 10K	Have 27M hz CRYSTAL FB Aperture size 256MB 0X9E(Default , not Multi-GPU usage) VGA Device

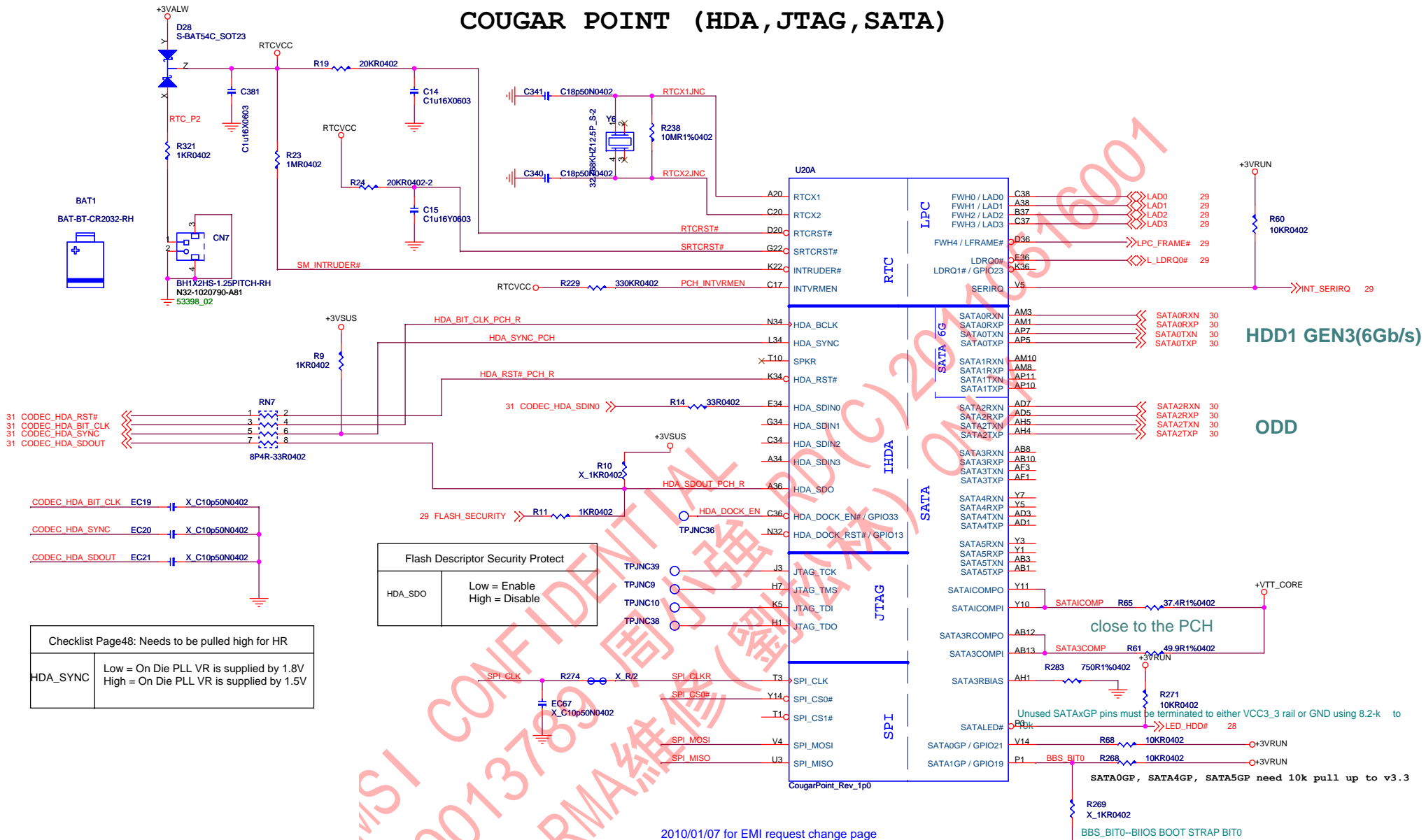
Rvalue	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



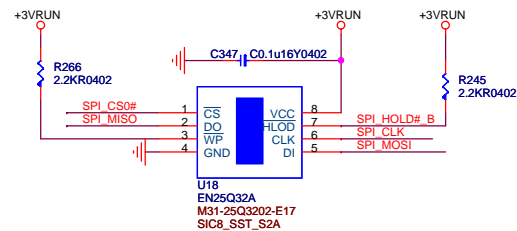




# COUGAR POINT (HDA, JTAG, SATA)

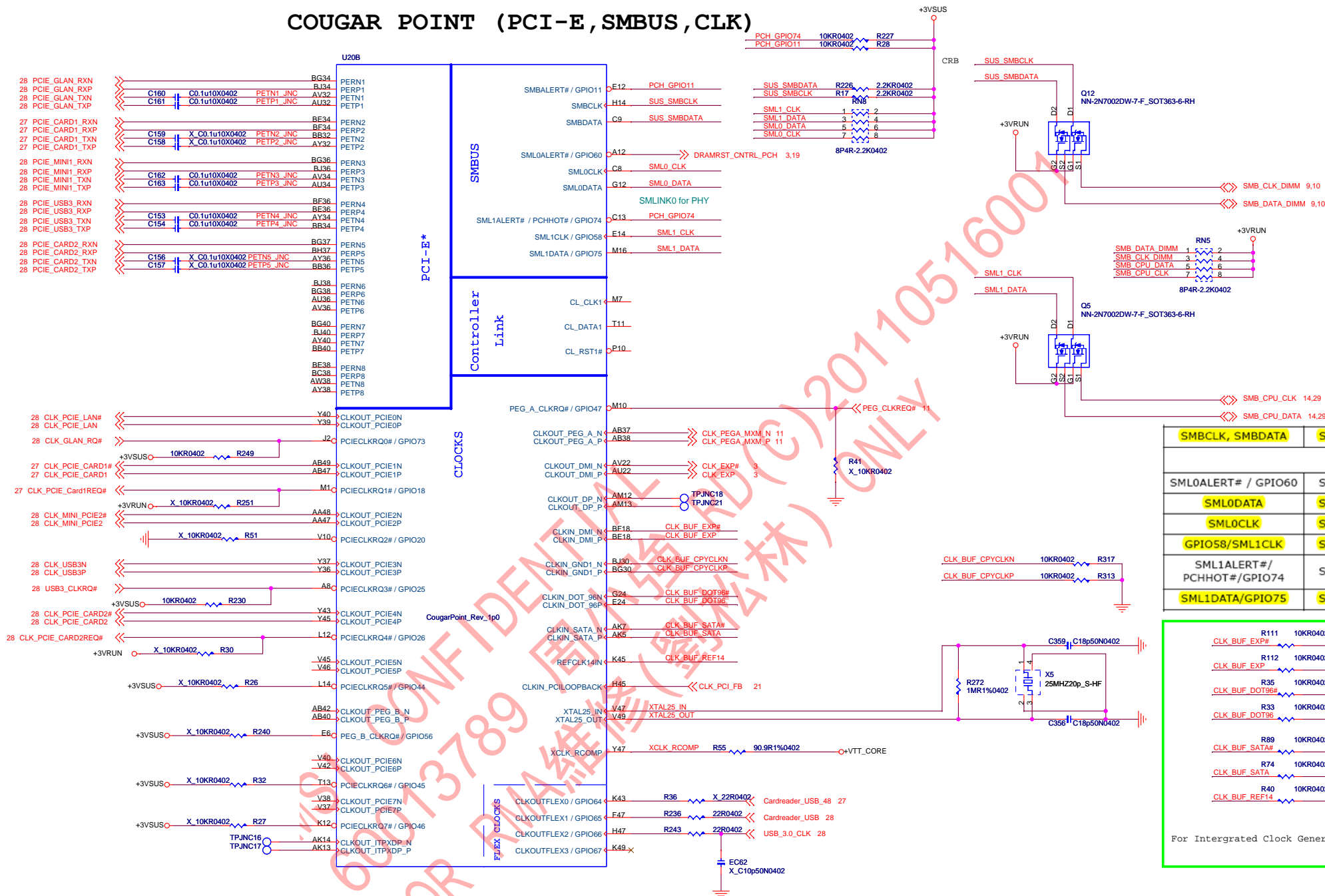


2010/01/07 for EMI request change page



Title		
PCH_HDA/JTAG/SATA		
Size	Document Number	Rev
Customer	MS-16G9/1754	0A
Date:	Tuesday, December 14, 2010	Sheet 17 of 52

## COUGAR POINT (PCI-E, SMBUS, CLK)

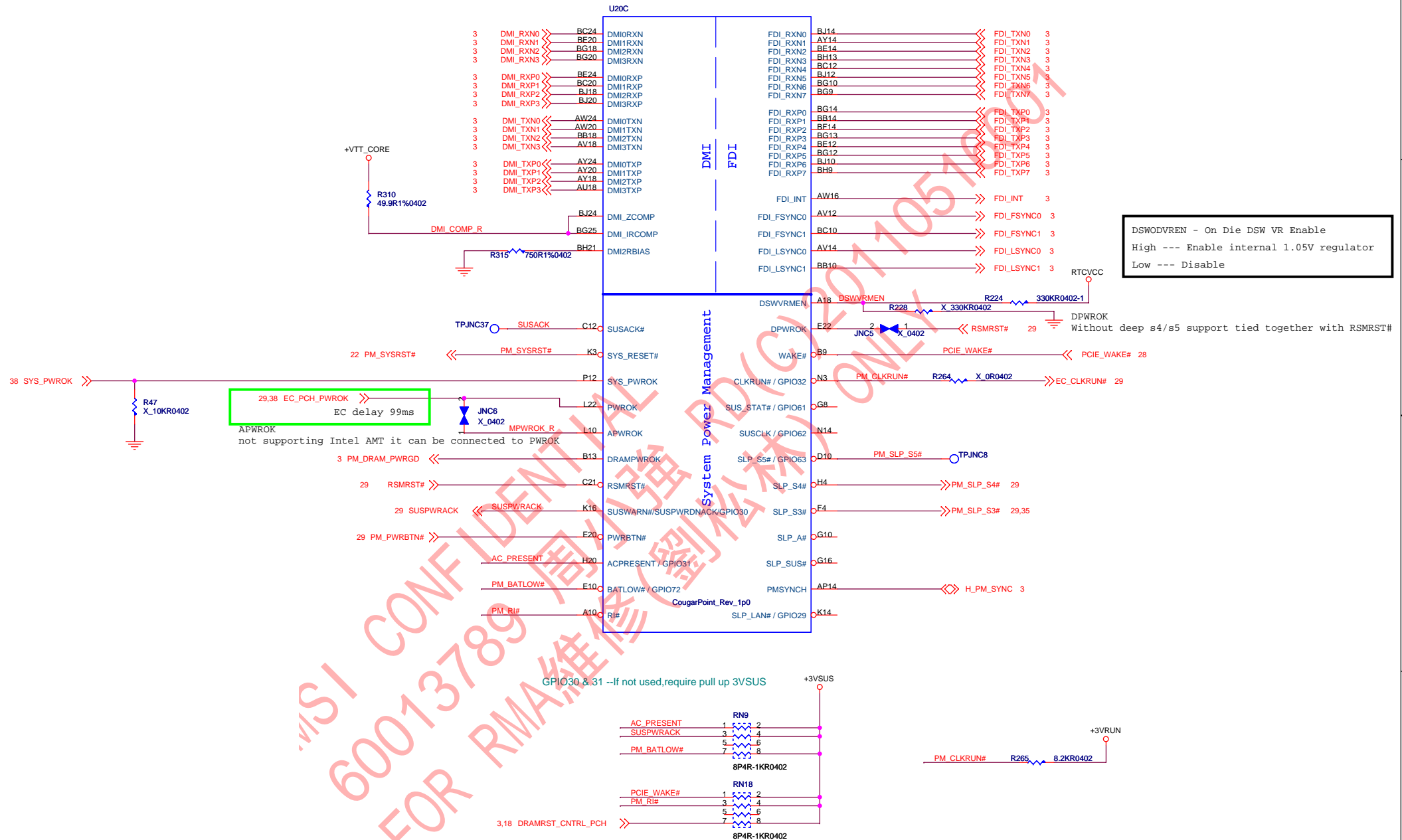


NOTE: If CLKREQ# control is not needed, say for a free running clock, do not pull-down signal to GND. This will increase leakage in Sx states. A 10 kohms±5% external pull-up resistor still needs to be used, but the corresponding CLKREQ# function can be disabled via Intel® Management Engine (Intel® ME) FW. Please refer to Intel ME FW Bring Up Guide for configuring/disabling CLKREQ#.

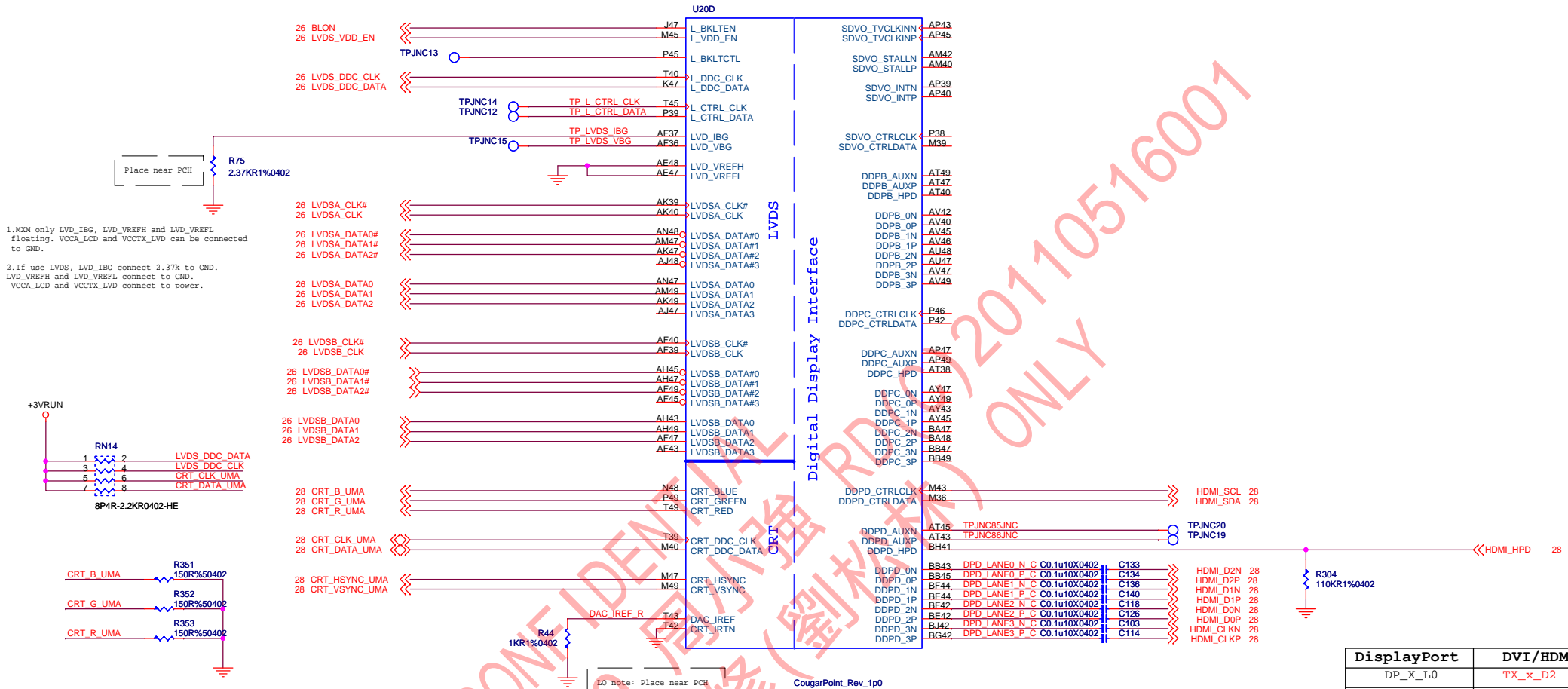
Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.

Title									
<b>PCH_PCIE/SMBUS/CLK</b>									
Size	Document Number								Rev
Customer	<b>MS-16G9/1754</b>								<b>0A</b>
Date:	Tuesday, December 14, 2010				Sheet	18	of	52	

## COUGAR POINT (DMI, FDI, GPIO)



# COUGAR POINT (LVDS,DDI)

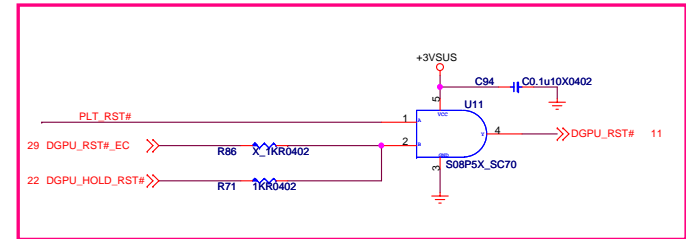
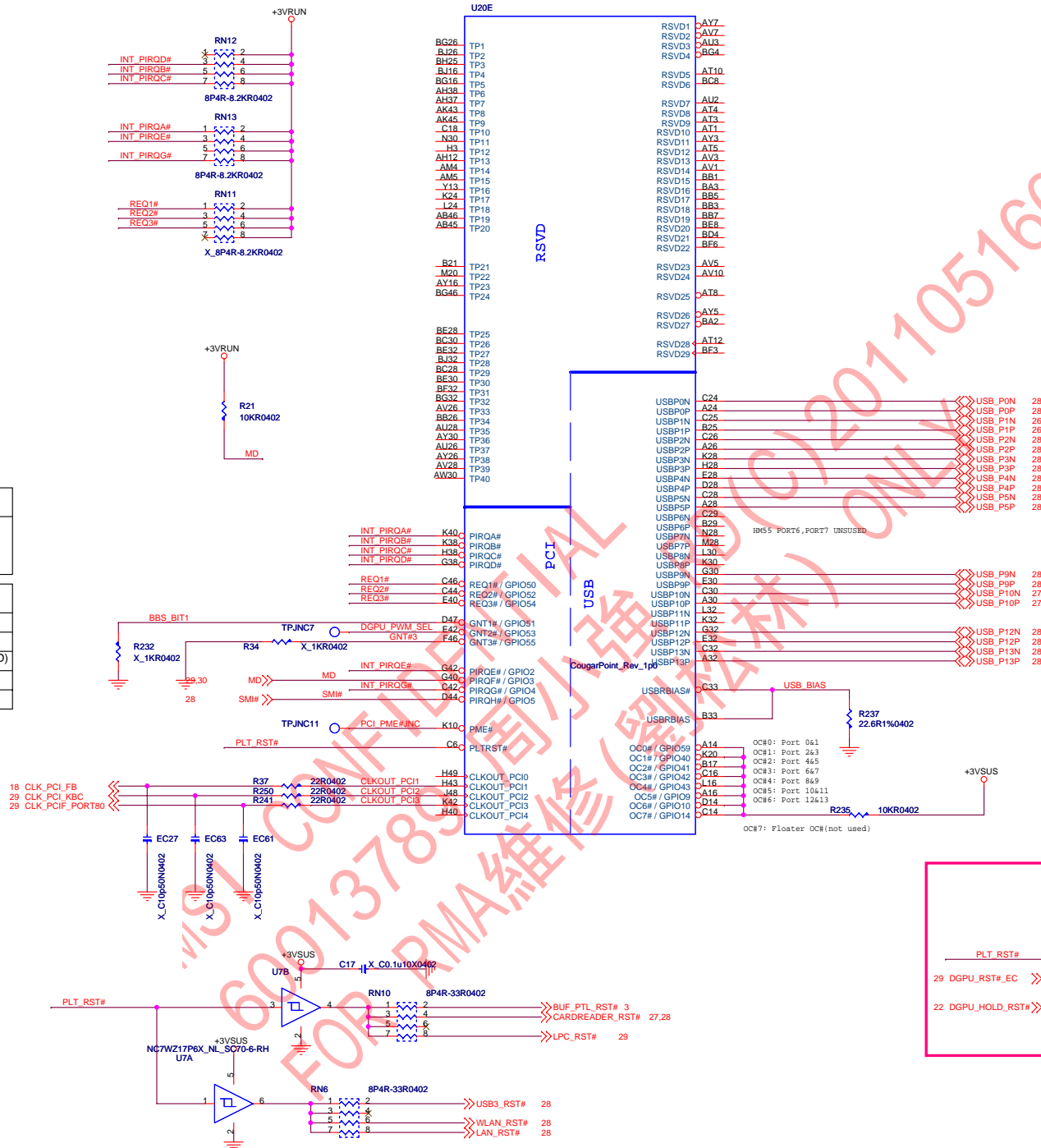


DisplayPort	DVI/HDMI
DP_X_L0	TX_x_D2
DP_X_L0#	TX_x_D2#
DP_X_L1	TX_x_D1
DP_X_L1#	TX_x_D1#
DP_X_L2	TX_x_D0
DP_X_L2#	TX_x_D0#
DP_X_L3	TX_x_CLK
DP_X_L3#	TX_x_CLK#
DP_X_AUX	DDC_x_CLK
DP_X_AUX#	DDC_x_DATA

# COUGAR POINT (PCI,USB,NVRAM)

A16 swap override Strap/Top-Block Swap Override jumper	
GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	-
1	1	SPI



GPIO0 & 6 & 16 & 22 & 34 & 38 & 48 --If not used,require pull up 3VRUN  
GPIO57 --If not used,require pull up 3VSUS  
GPIO15--High is support TLS,internal pull-down  
GPIO27 is deep S4 & S5 weak up event,internal pull high.& It's VCCFDIPLL internal VRM strapping pin  
GPIO35 --Un- Muxed. If not used Can be NC

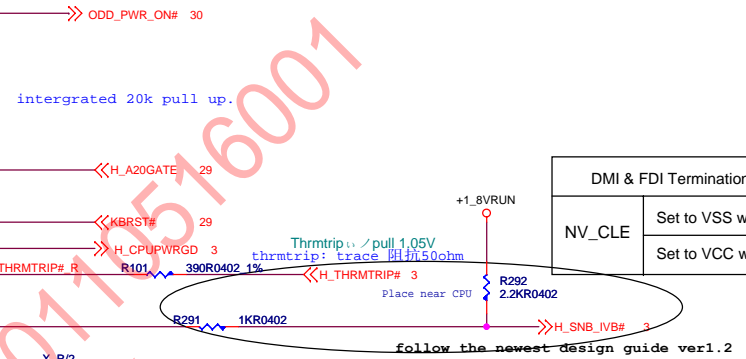
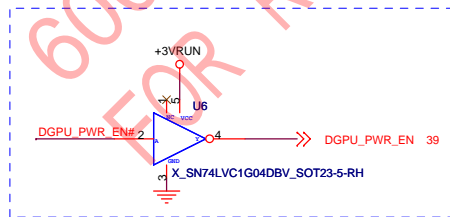
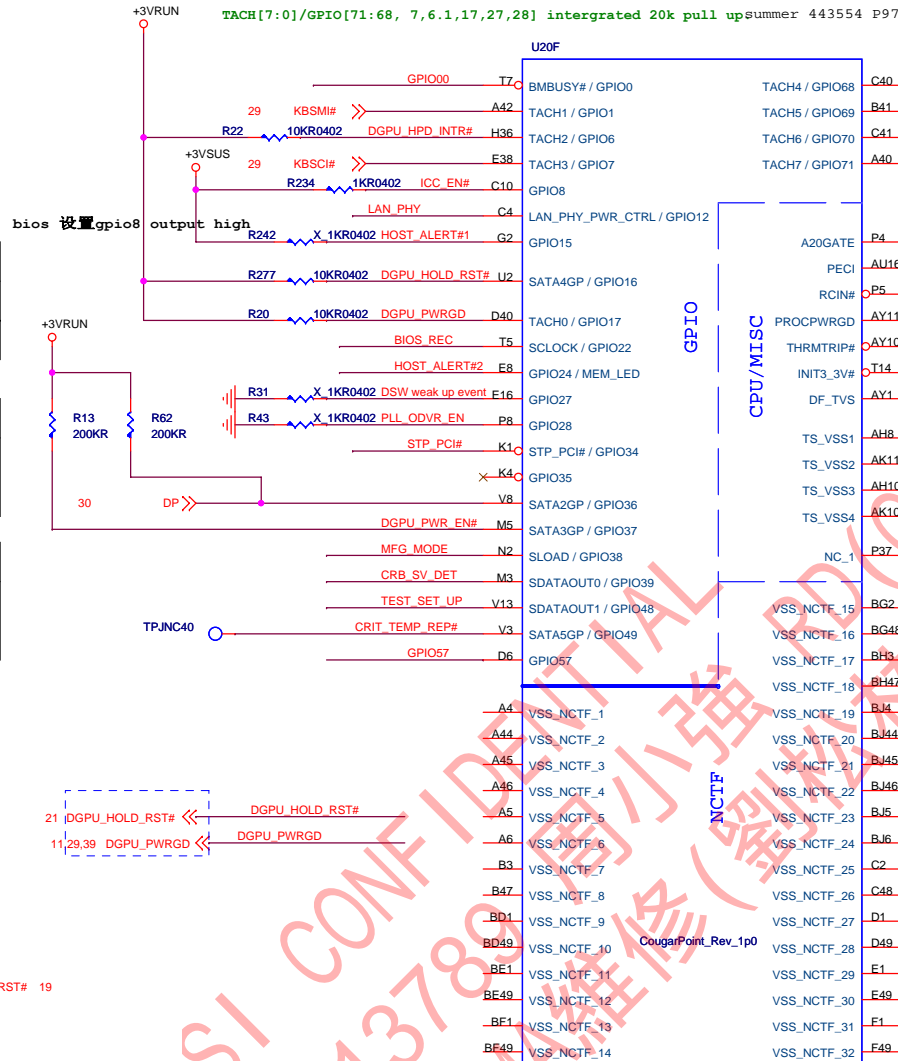
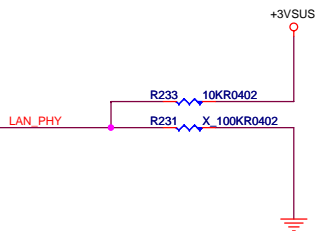
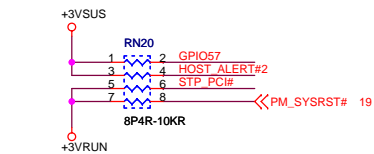
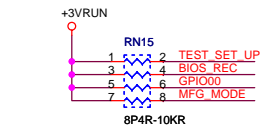
## COUGAR POINT (GPIO,VSS\_NCTF,RSVD)

GPIO8 is no longer needed as a functional strap for Integrated clocking. Integrated Clock Enable functionality is achieved via soft-strap. The current default is Clock Enabled.

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable) Low: Disable

DMI termination voltage override	
GPIO36	Low-- TX,RX terminated to same voltage (DC coupling mode)default

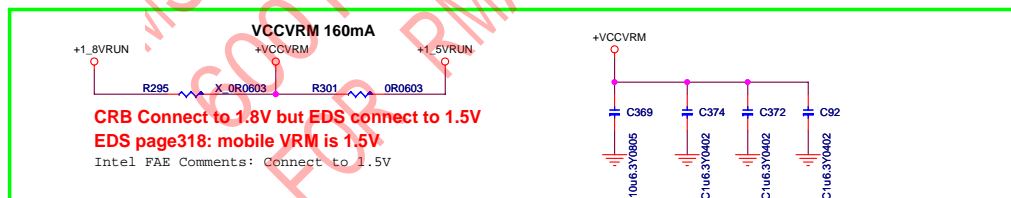
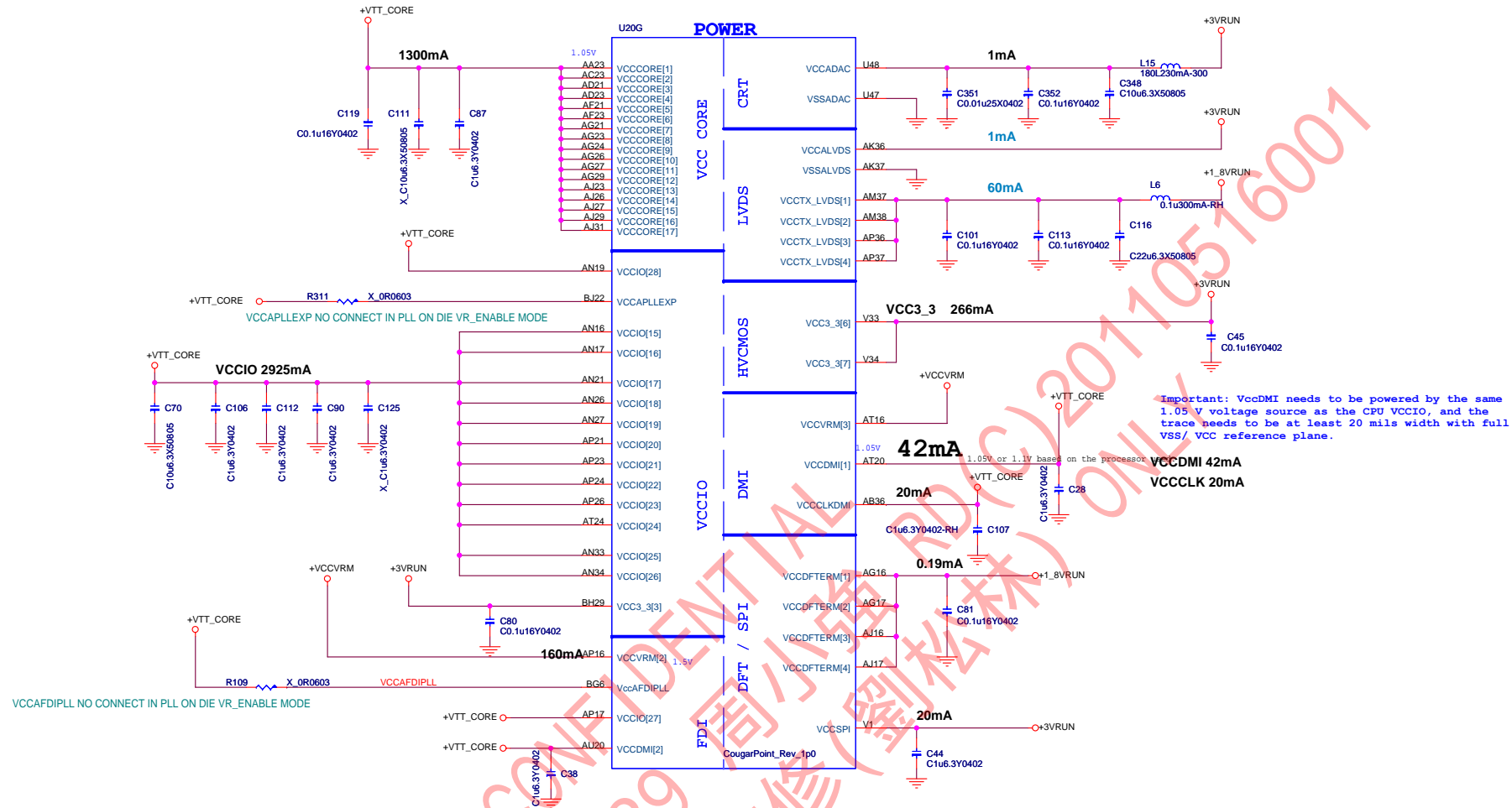
FDI termination voltage override	
GPIO37	Low-- TX,RX terminated to same voltage (DC coupling mode)default



Intel Comments:  
Reserve 0 ohm option in these pins  
pins AH8, AK11, AH10 & AK10) to GND.  
These signals should not float on the motherboard. They should be  
tied to GND directly.

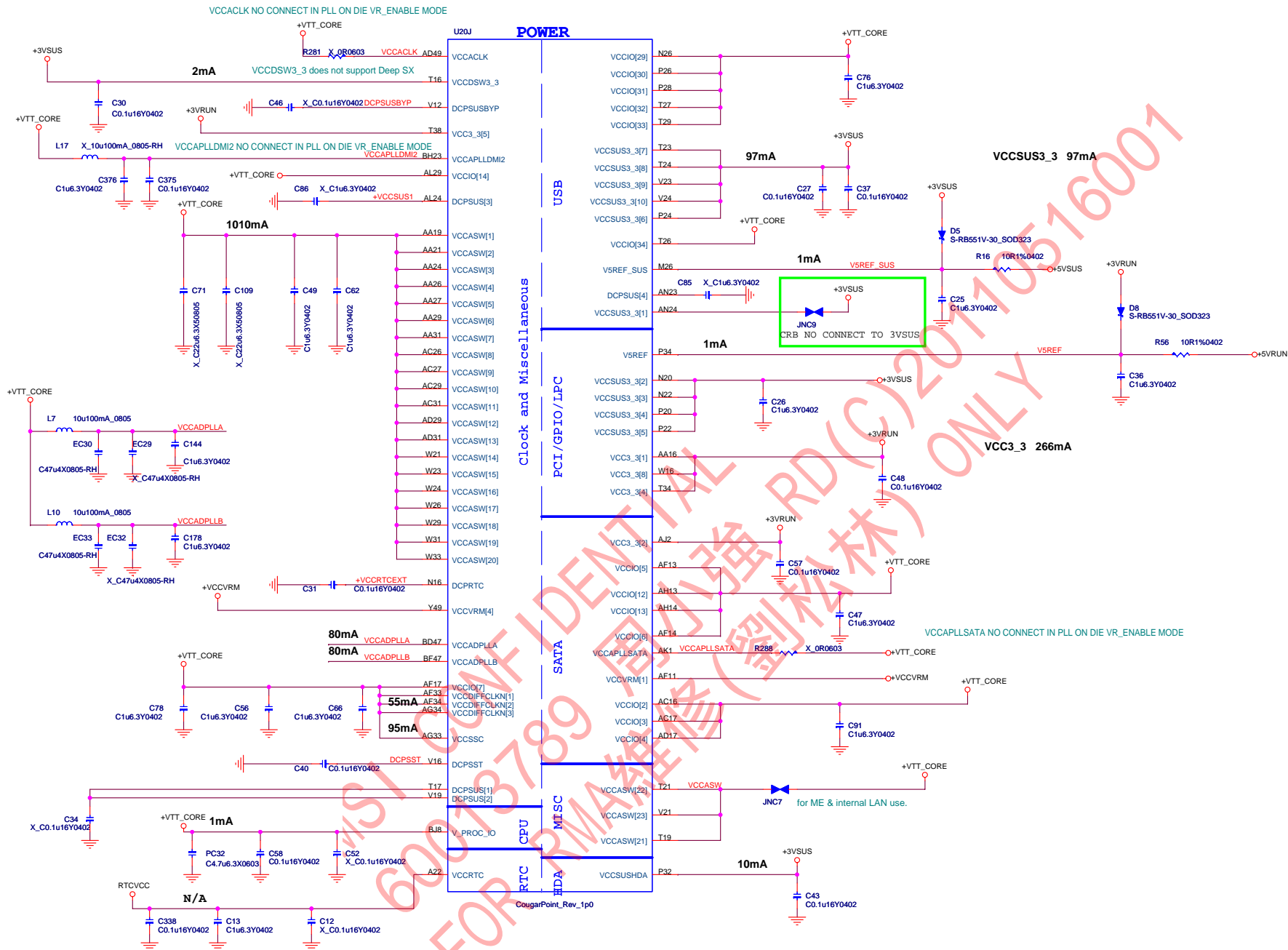
CRB_SV_DET	
GPIO39	High: External GFX Low: Internal GFX

## COUGAR POINT (POWER)



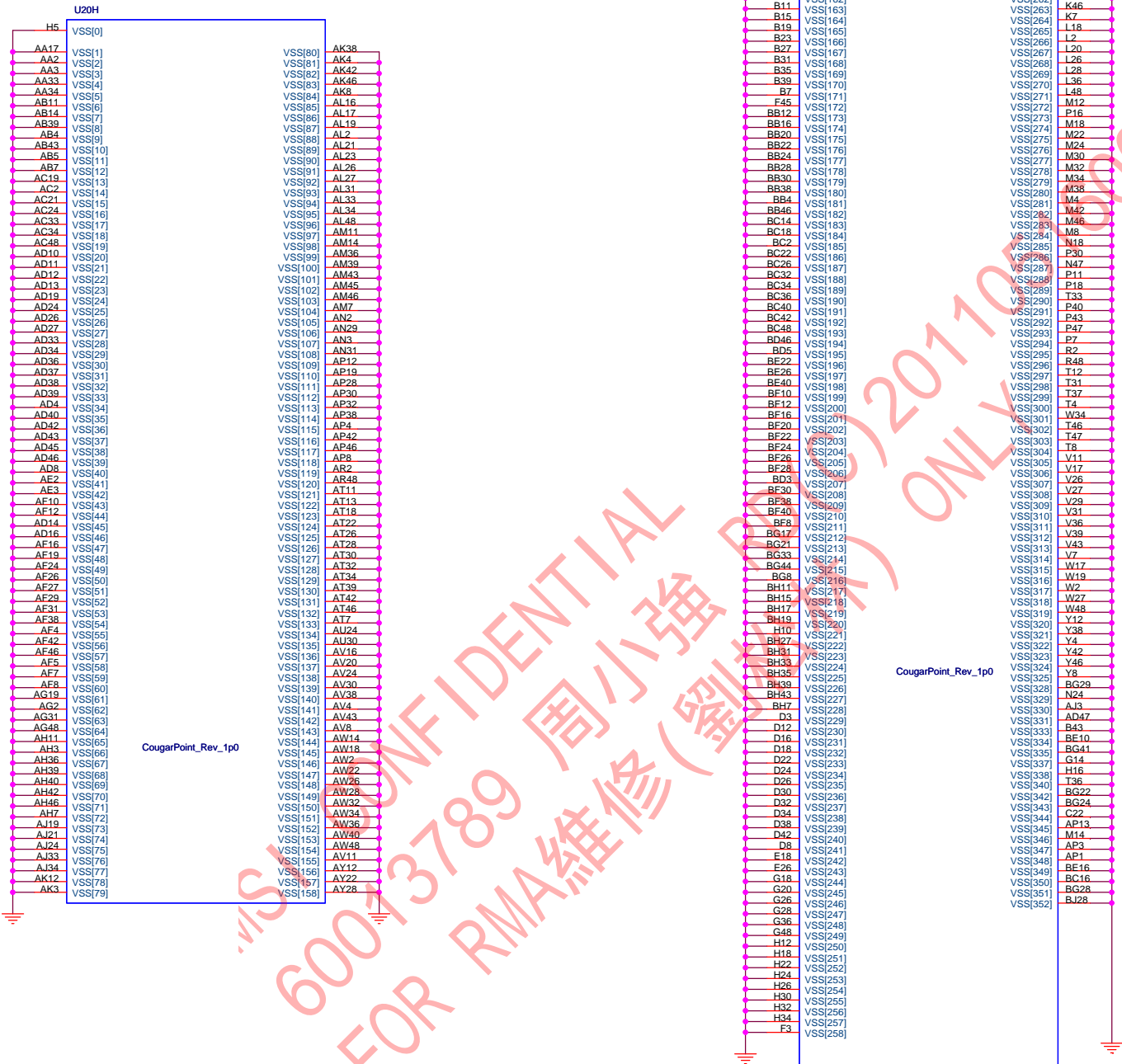


## COUGAR POINT (POWER)

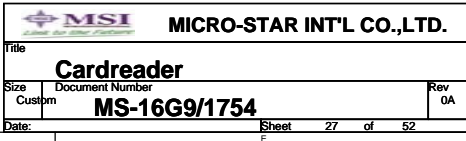


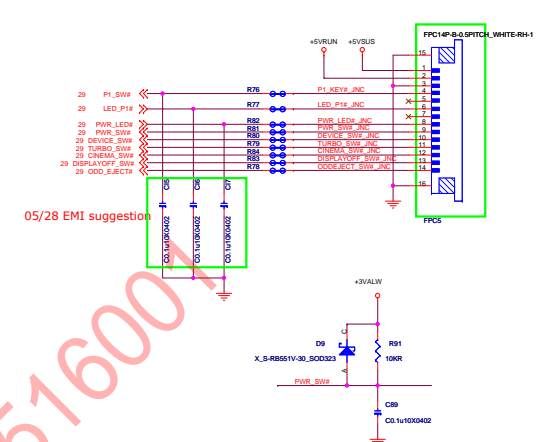
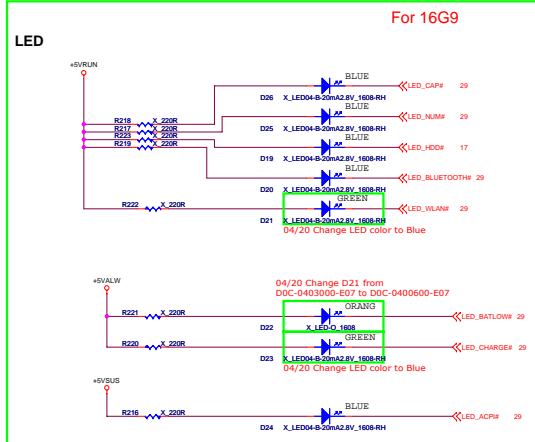
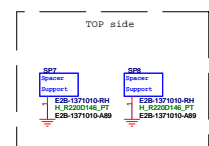
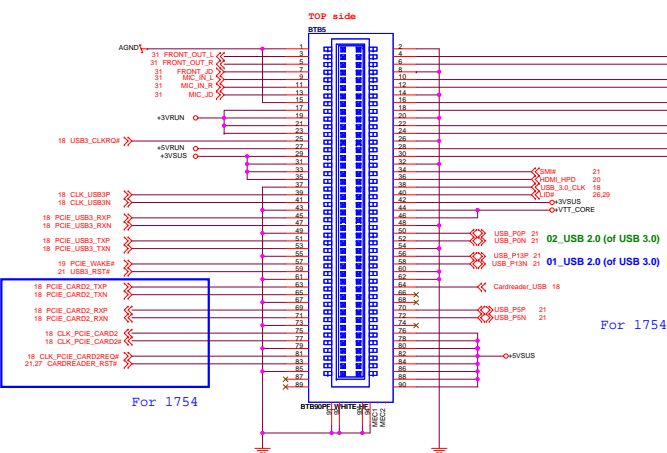


Cougar Point (GND)

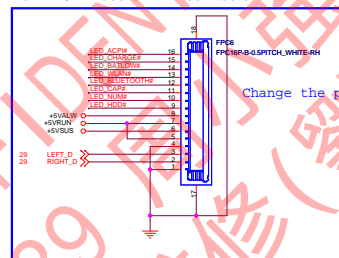


Title				
CRT/LVDS/CCD				
Size	Document Number			Rev
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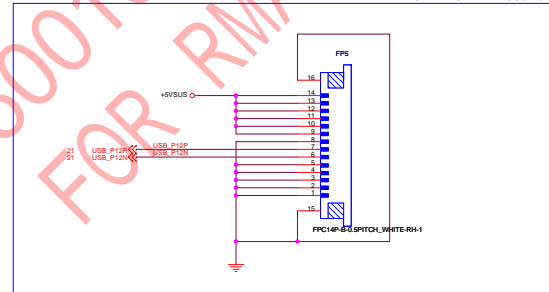


For 1754 E board LED connector

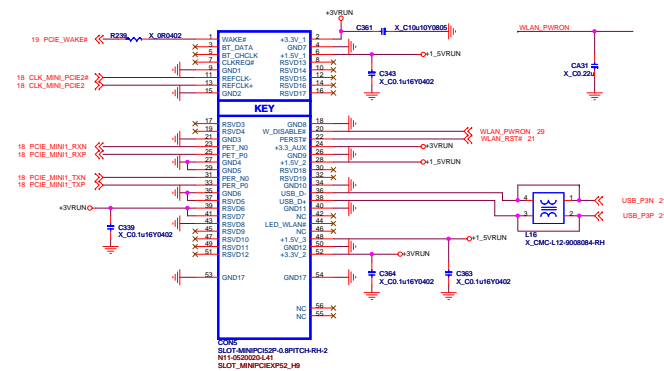


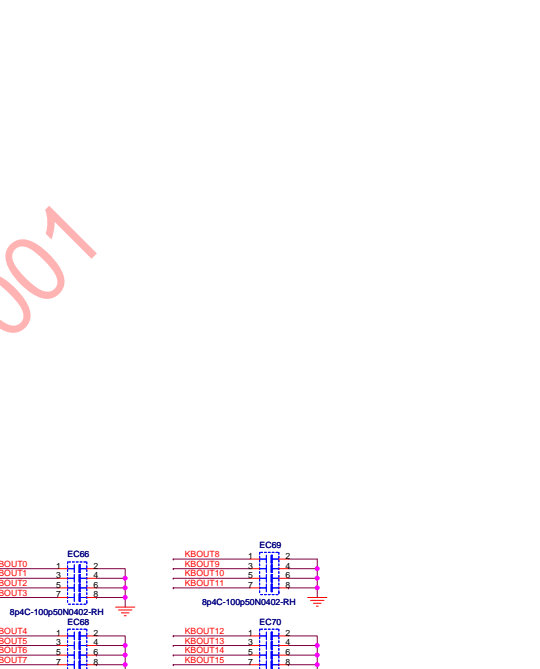
Change the pin define 0824!

For 1754 D board connector



## WLAN





For 1754

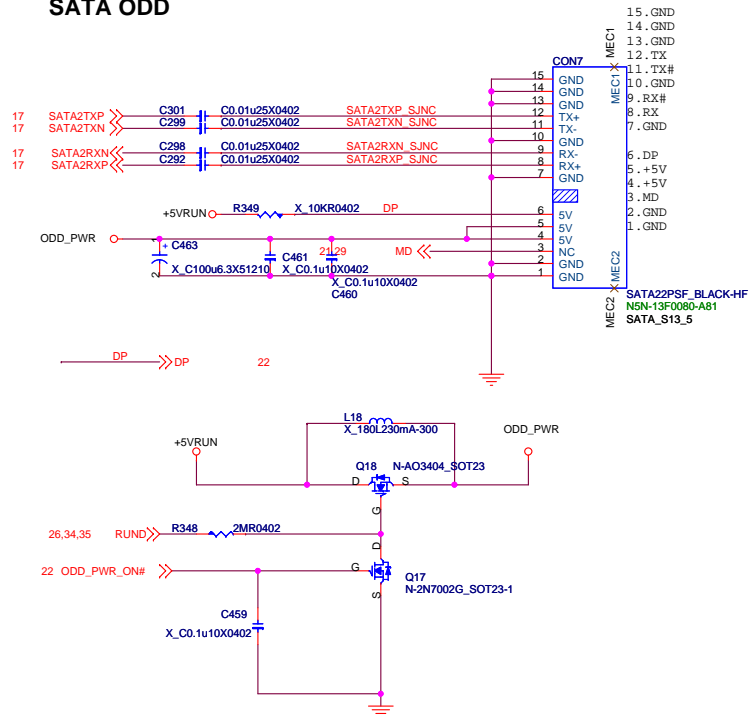
+5V/RUN

R159 X\_220R

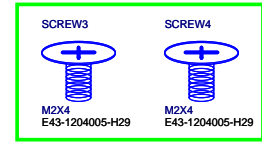
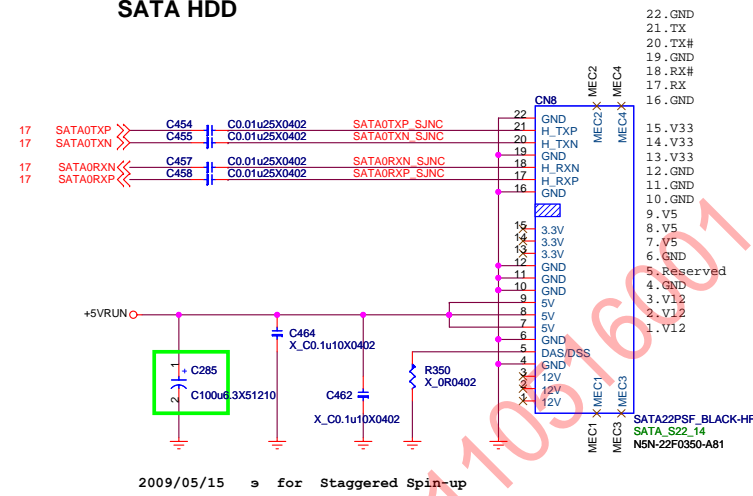
1 2 LED\_TP\_LOCK#

D16 X\_LED04-O 25mA2.4V\_20125-RH

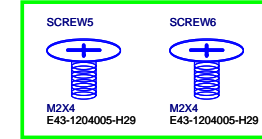
## SATA ODD



## SATA HDD

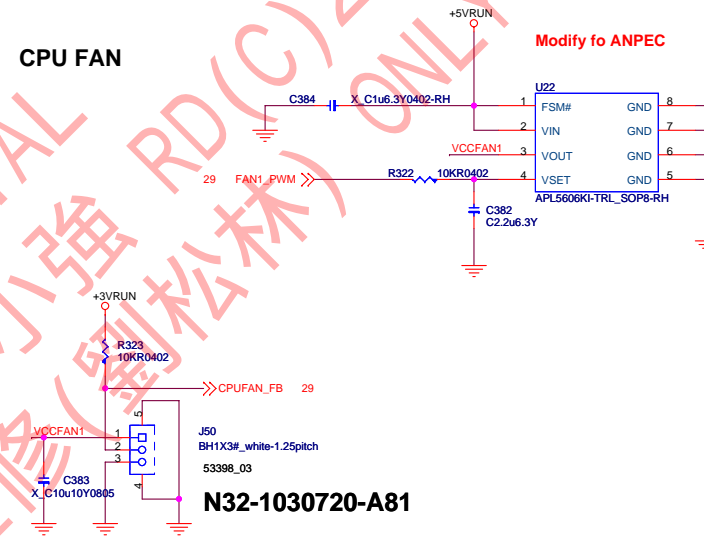


SCREW3,SCREW4 FOR HDD!

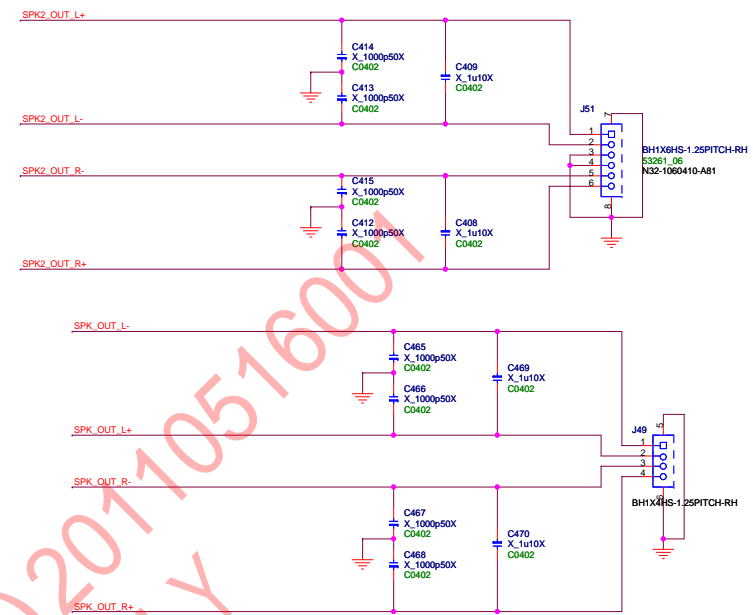


SCREW5,SCREW6 FOR ODD!

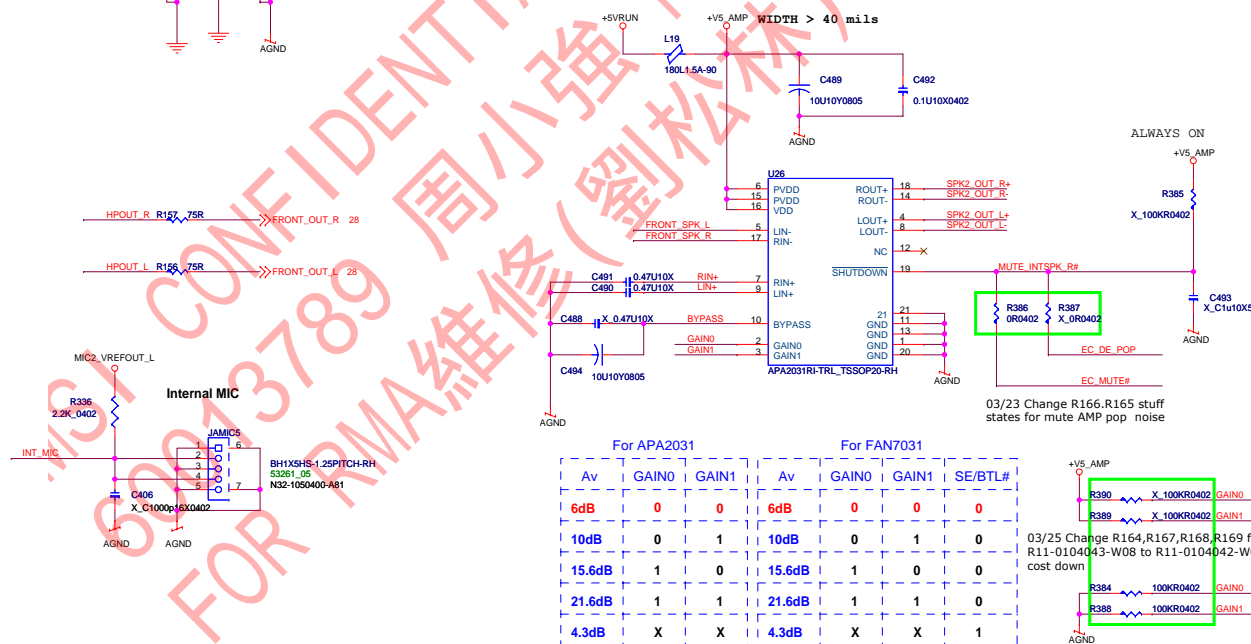
## CPU FAN



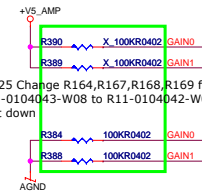
N32-1030720-A81



20 mil trace width is required for 4ohm loading  
10 mil trace width is required for 8ohm loading  
the trace length/ Speaker wire length of SPKL+/L-/R+/R- is same  
as possible as you can.

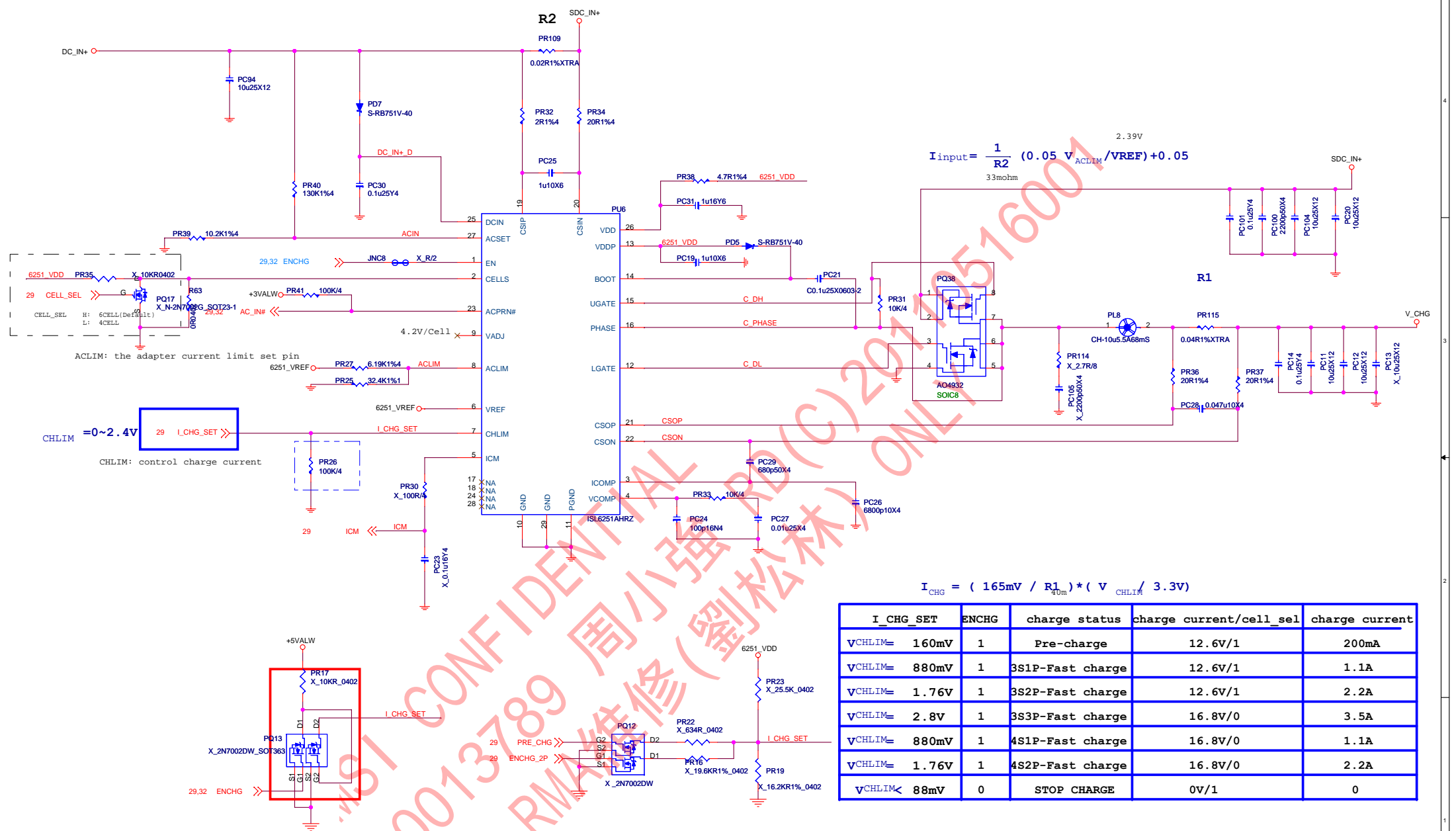


For APA2031			For FAN7031			
Av	GAIN0	GAIN1	Av	GAIN0	GAIN1	SE/BL
6dB	0	0	6dB	0	0	0
10dB	0	1	10dB	0	1	0
15.6dB	1	0	15.6dB	1	0	0
21.6dB	1	1	21.6dB	1	1	0
4.3dB	X	X	4.3dB	X	X	1









$$I_{input} = \frac{1}{R2} (0.05 V_{ACLIM} / VREF) + 0.05$$

$$I_{CHG} = (165mV / R1) * (V_{CHLIM} / 3.3V)$$

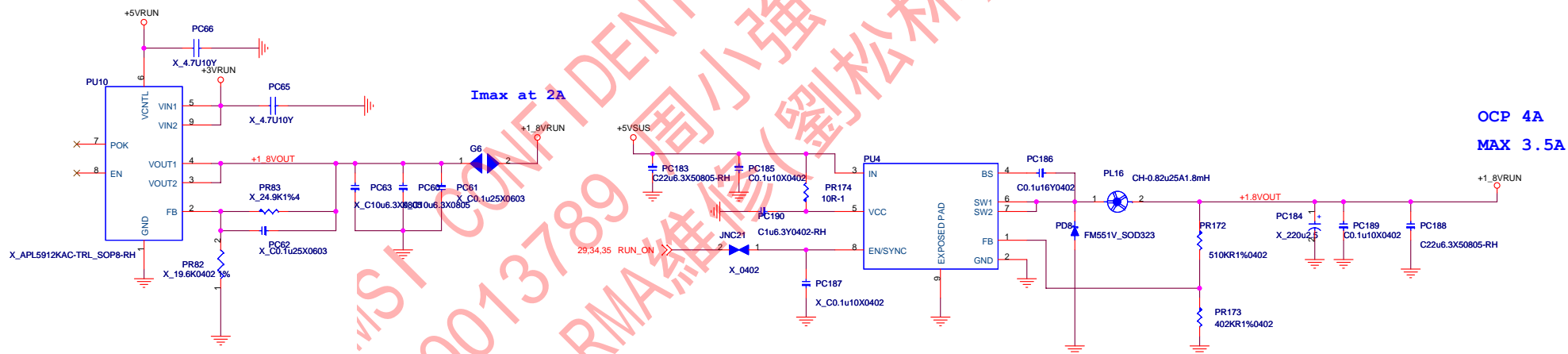
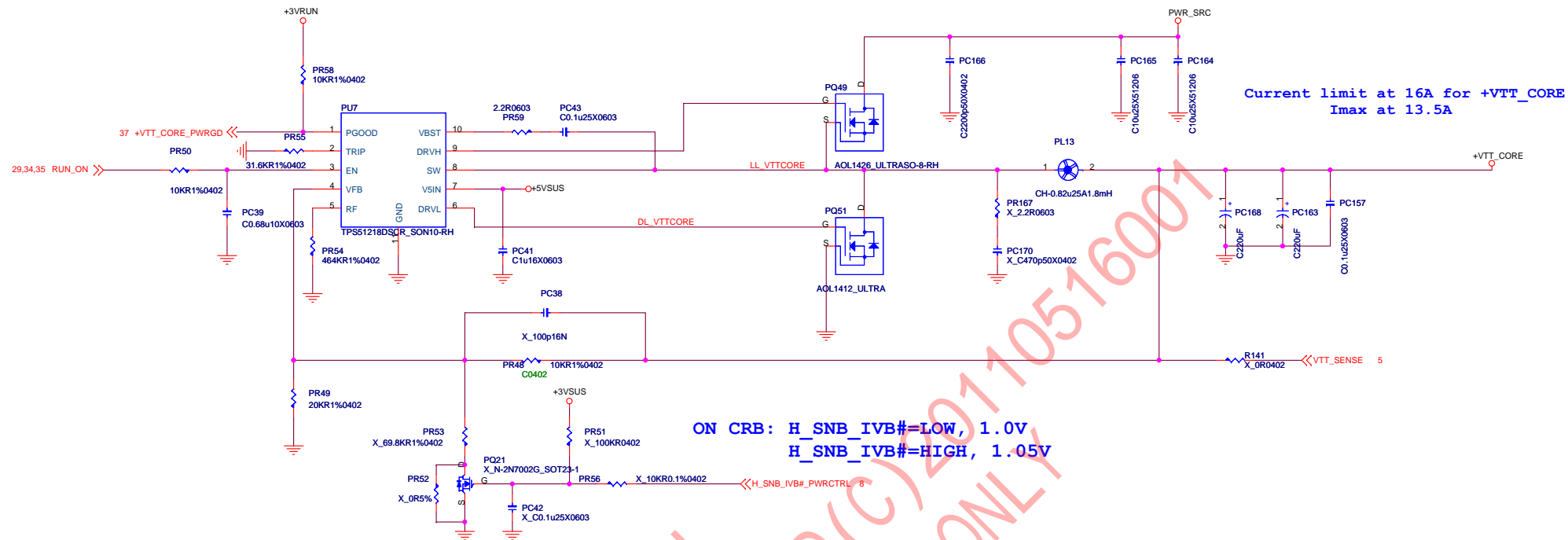
I_CHG_SET	ENCHG	charge status	charge current/cell_sel	charge current
VCHLIM= 160mV	1	Pre-charge	12.6v/1	200mA
VCHLIM= 880mV	1	3S1P-Fast charge	12.6V/1	1.1A
VCHLIM= 1.76V	1	3S2P-Fast charge	12.6V/1	2.2A
VCHLIM= 2.8V	1	3S3P-Fast charge	16.8V/0	3.5A
VCHLIM= 880mV	1	4S1P-Fast charge	16.8V/0	1.1A
VCHLIM= 1.76V	1	4S2P-Fast charge	16.8V/0	2.2A
VCHLIM< 88mV	0	STOP CHARGE	0V/1	0

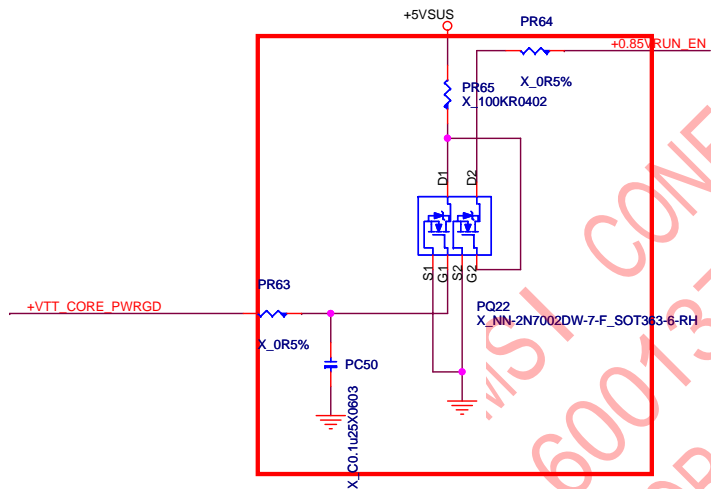
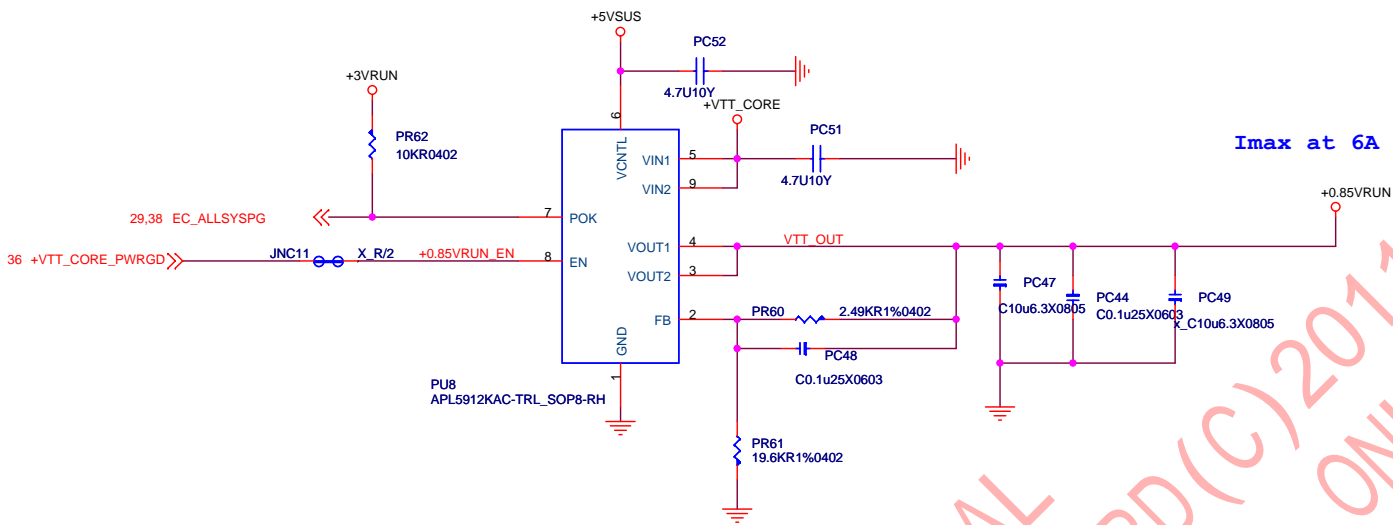
Current limit at 7A for +3VSUS  
Imax at 6A

Current limit at 8A for +5VSUS  
Imax at 7A

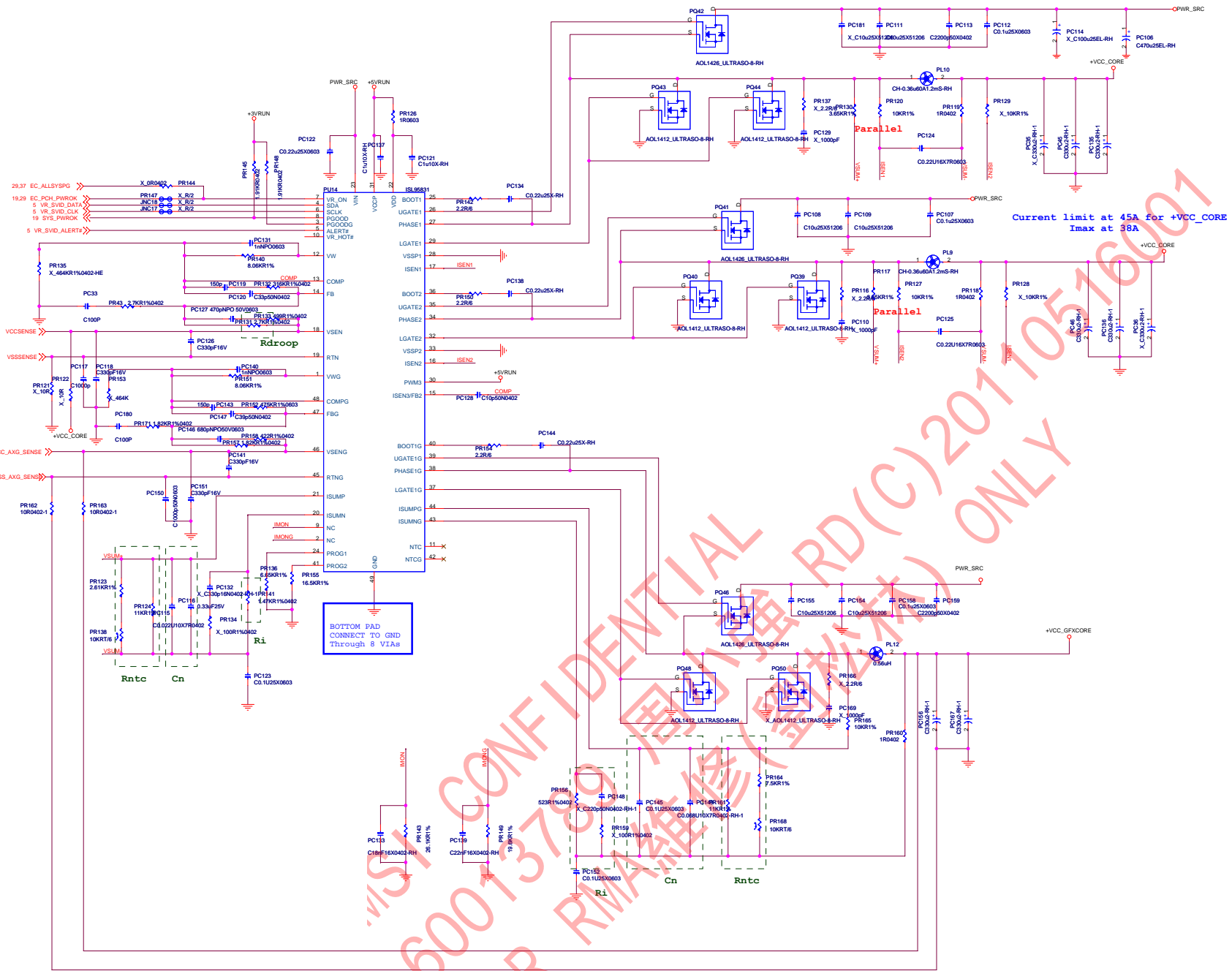
Title			System Power
Size	Document Number		
Customer	MS-16G9/1754	Rev	0A
Date:	Tuesday, December 14, 2010	Sheet	34 of 52

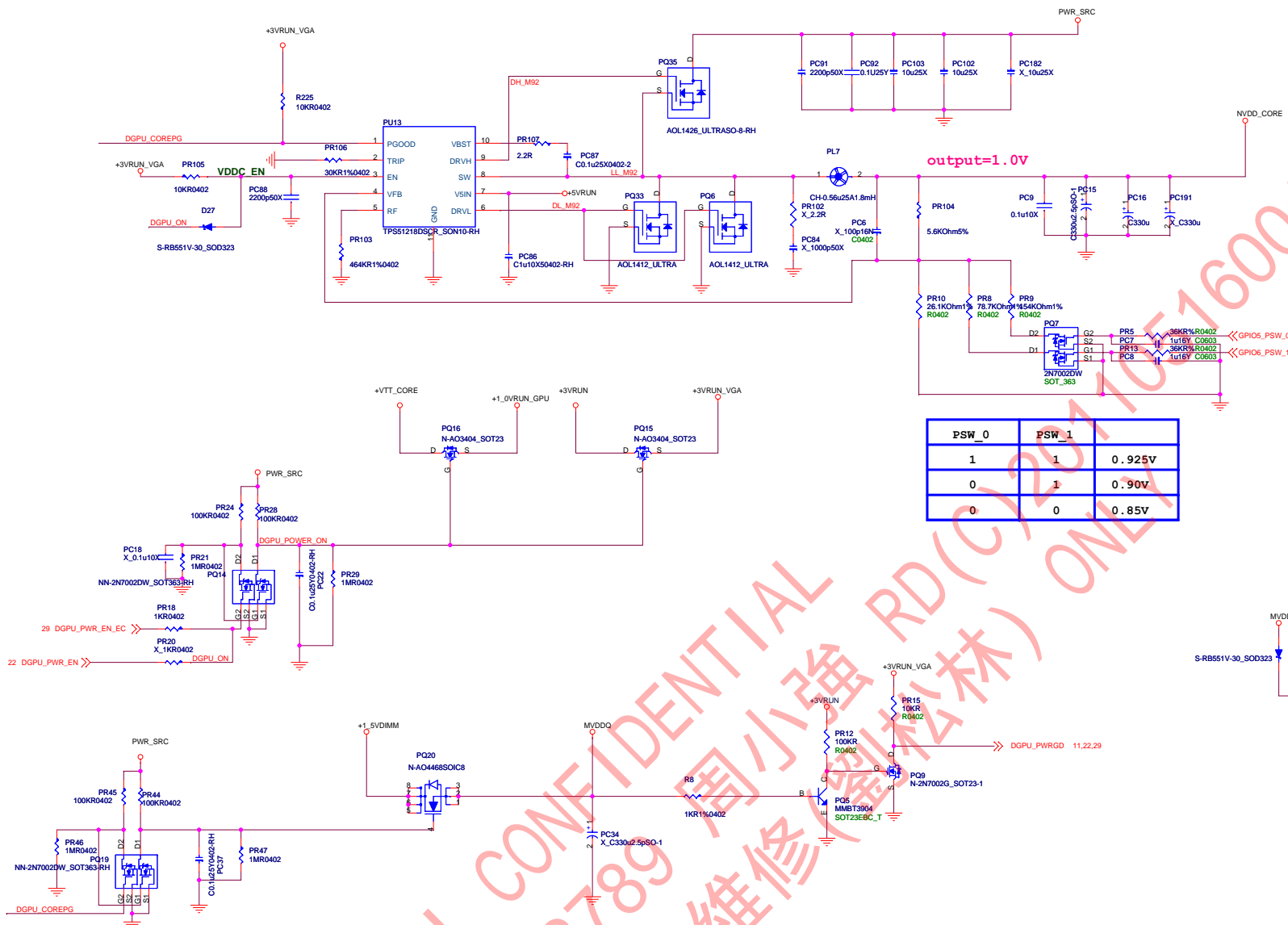






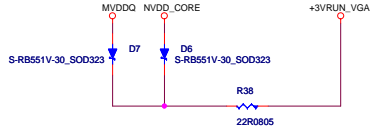
Title			0.85V
Size B	Document Number		Rev 0A
		MS-16G9/1754	
Date:	Tuesday, December 14, 2010	Sheet 37 of 52	



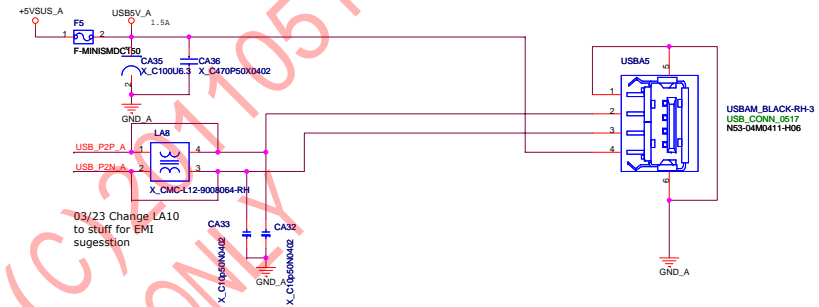
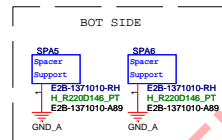
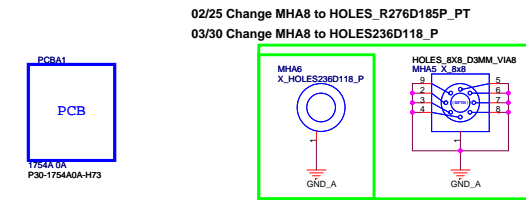
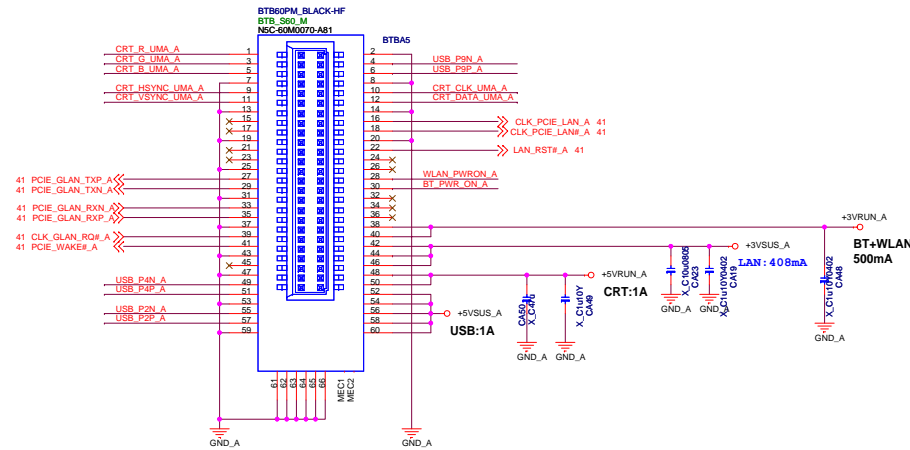


PSW_0	PSW_1	
1	1	0.925V
0	1	0.90V
0	0	0.85V

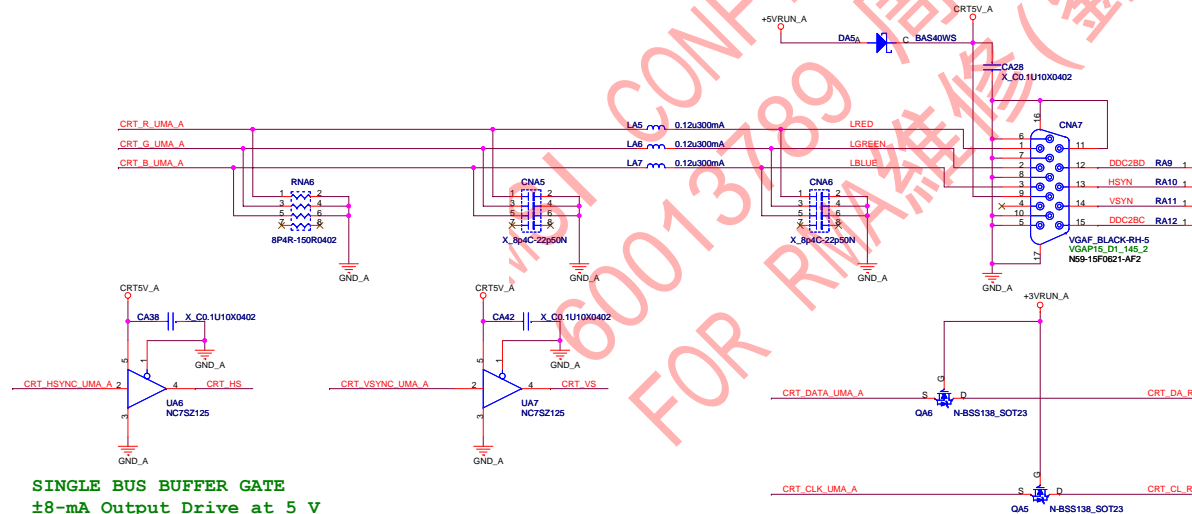
Imax= 16A  
Iocp=20.8A



( ESATA,USB,LAN,CRT,BT+WLAN)

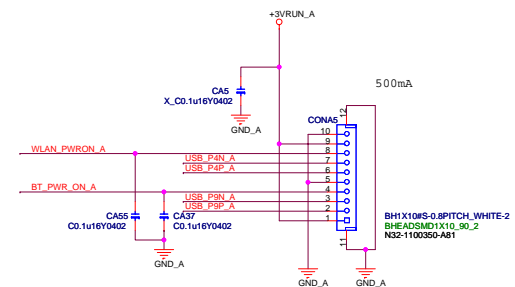


## D-Sub Connector



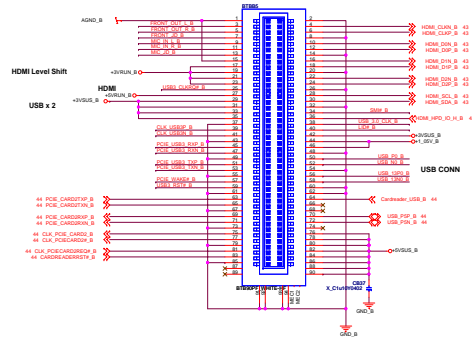
SINGLE BUS BUFFER GATE  
±8-mA Output Drive at 5 V

## BT and WLAN Combo Connector

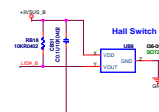




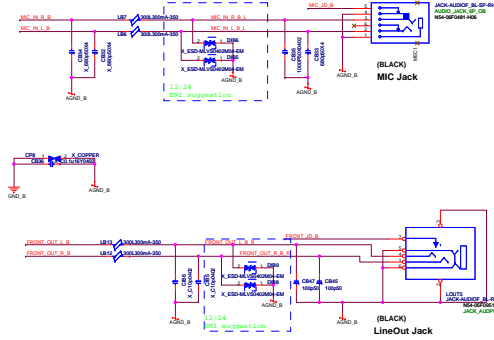




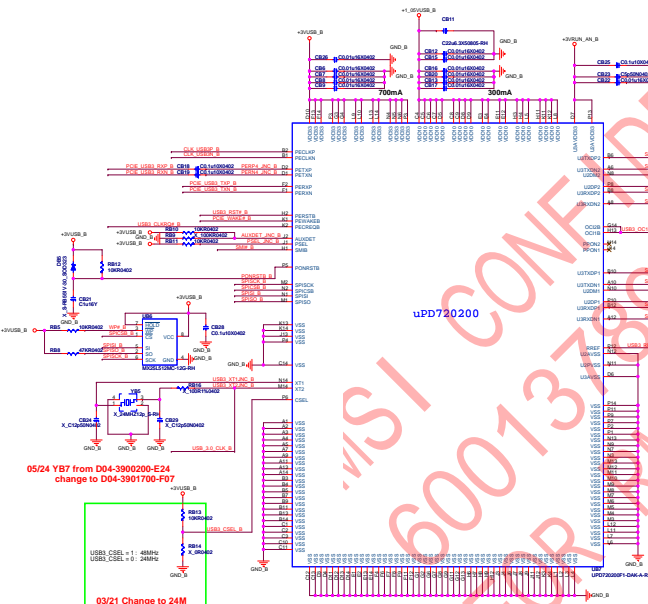
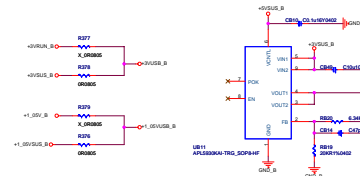
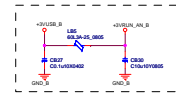
# LID Switch



# Audio Jack



# (才四Card reader,USB 3.0 x 2) USB 3.0 Connector

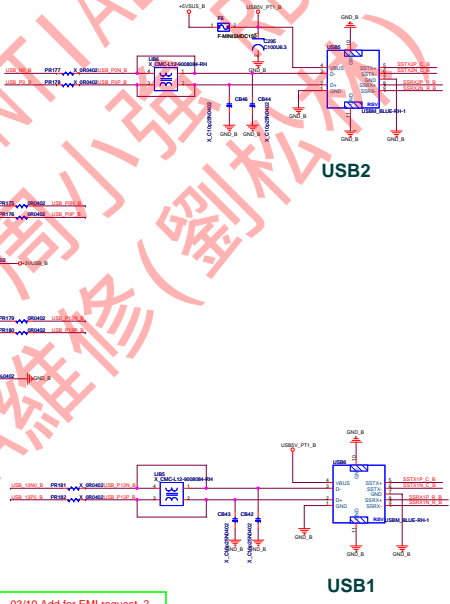


05/24 Y87 from D04-3900200-E24  
change to D04-3901700-F07

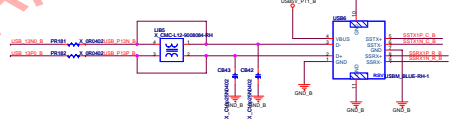
03/21 Change to 24M

03/19 Add for EMI request ?

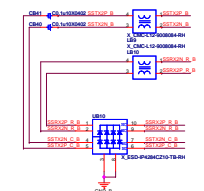
# USB2



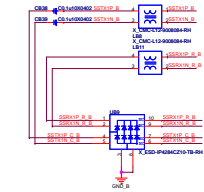
# USB1



# 04/14 LB21, LB18 SWAP PIN



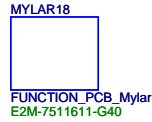
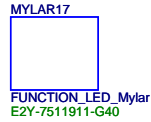
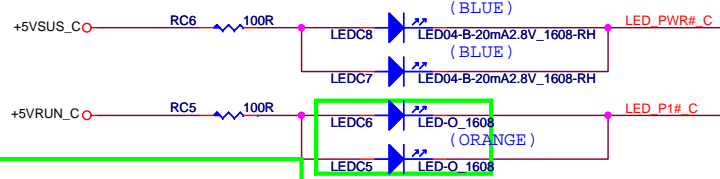
# 04/14 LB19, LB20 SWAP PIN



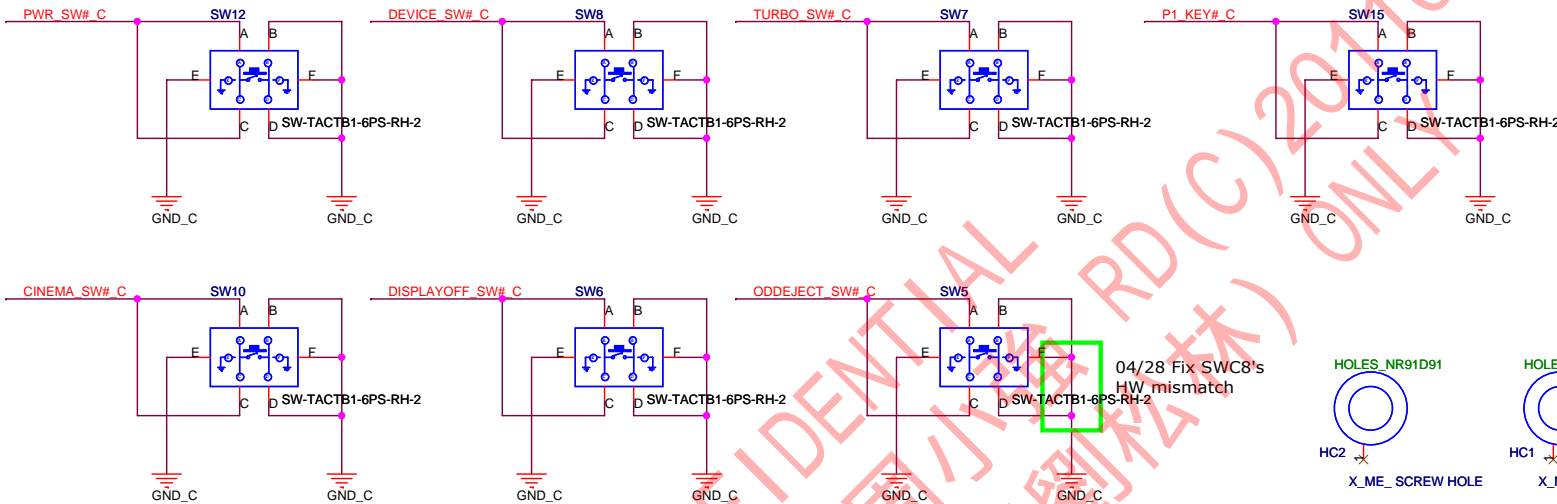




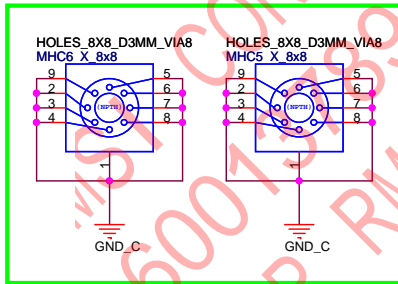
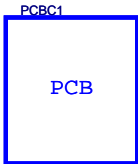
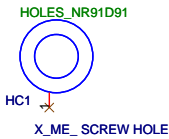
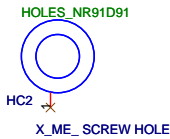
03/30 Change LEDC7.LEDC8 from  
D0C-04018F0-L05 to  
D0C-0400600-E07



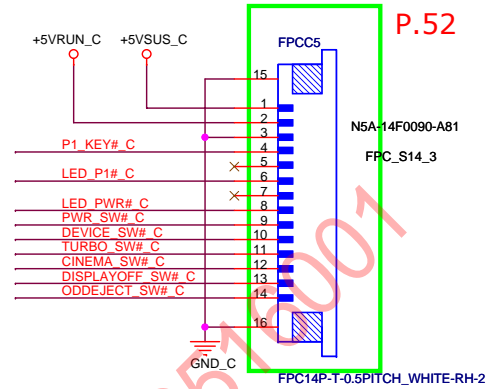
03/29 Remove ECO and Cinema LED for ID request



04/28 Fix SWC8's  
HW mismatch

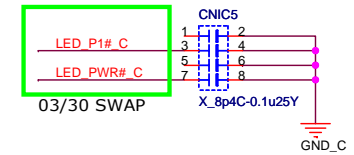


02/10 Add 8 vias for EMI suggestion

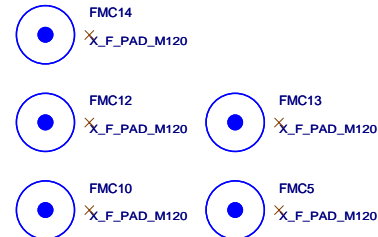
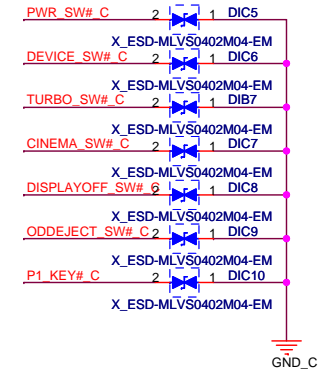



P.52

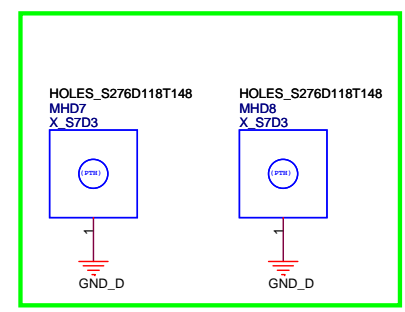
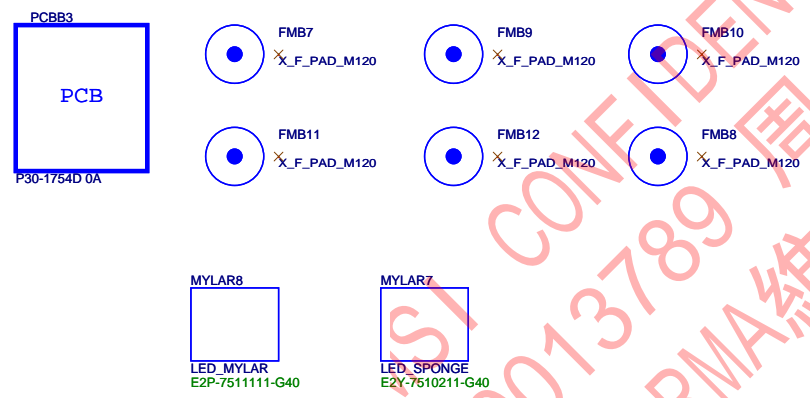
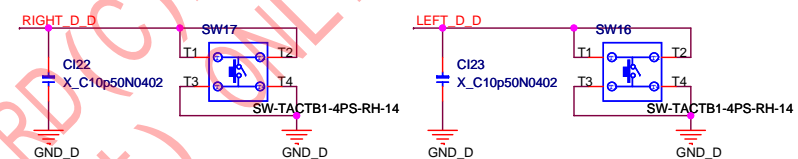
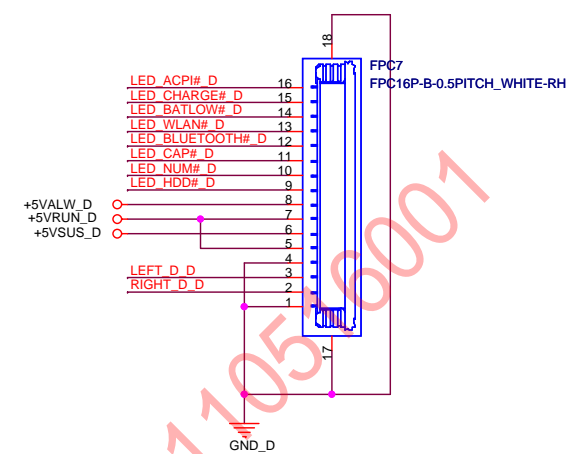
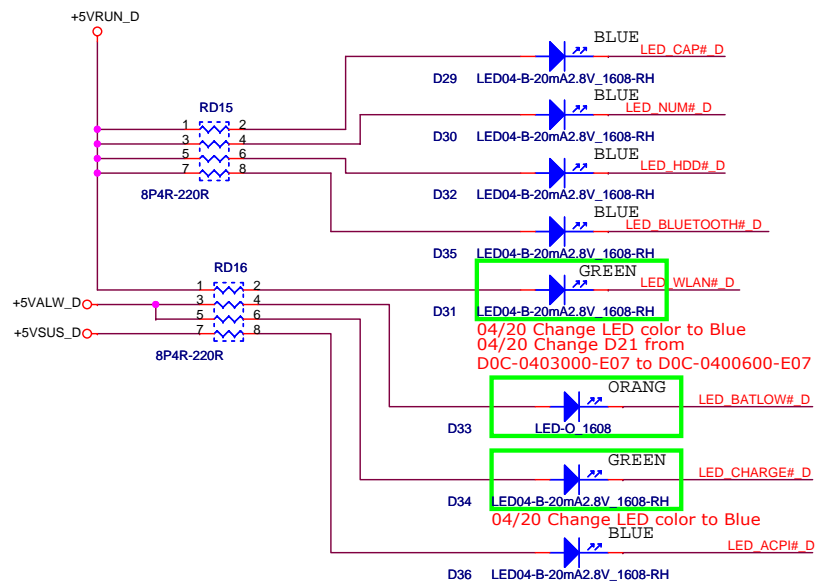
04/23 Change FPC7 from N5A-14F0070-A81 to  
N5A-14F0090-A81(P/N only) for ME request



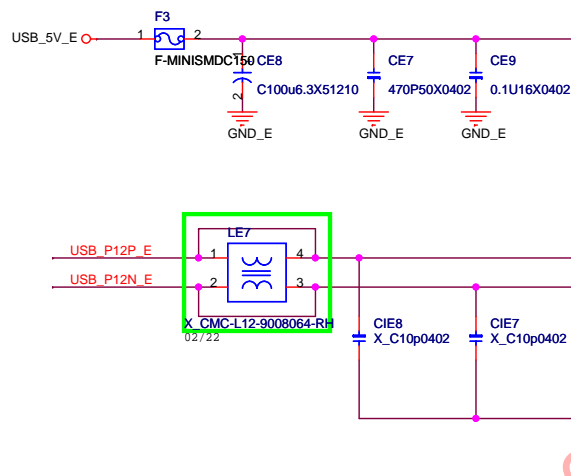
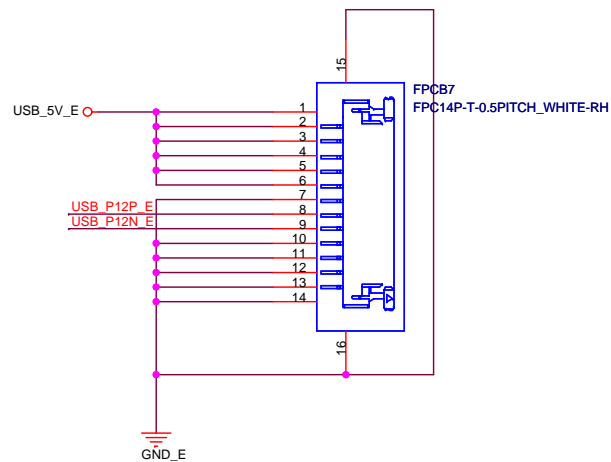
03/30 SWAP



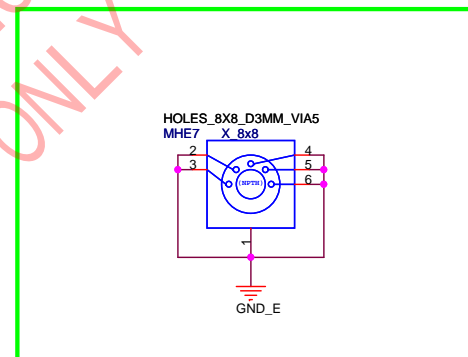
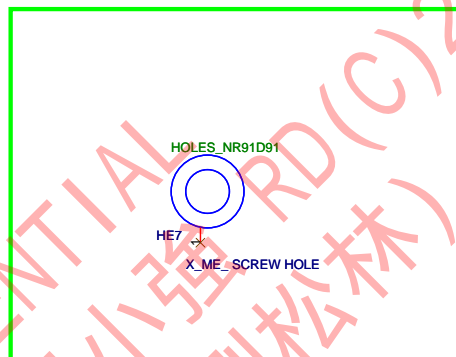
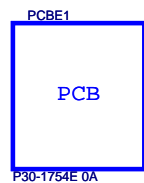
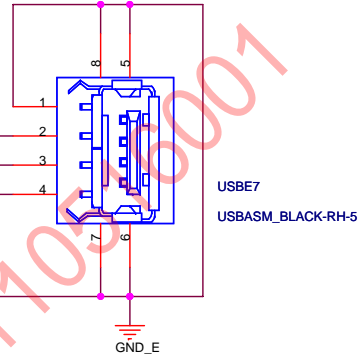
 <b>MICRO-STAR INT'L CO.,LTD.</b>		
<b>Title</b> PWR SW / LED		
<b>Size</b> B	<b>Document Number</b> MS-16G9/1754	<b>Rev</b> 0A
<b>Date:</b>	<b>Sheet</b> 45	<b>of</b> 52




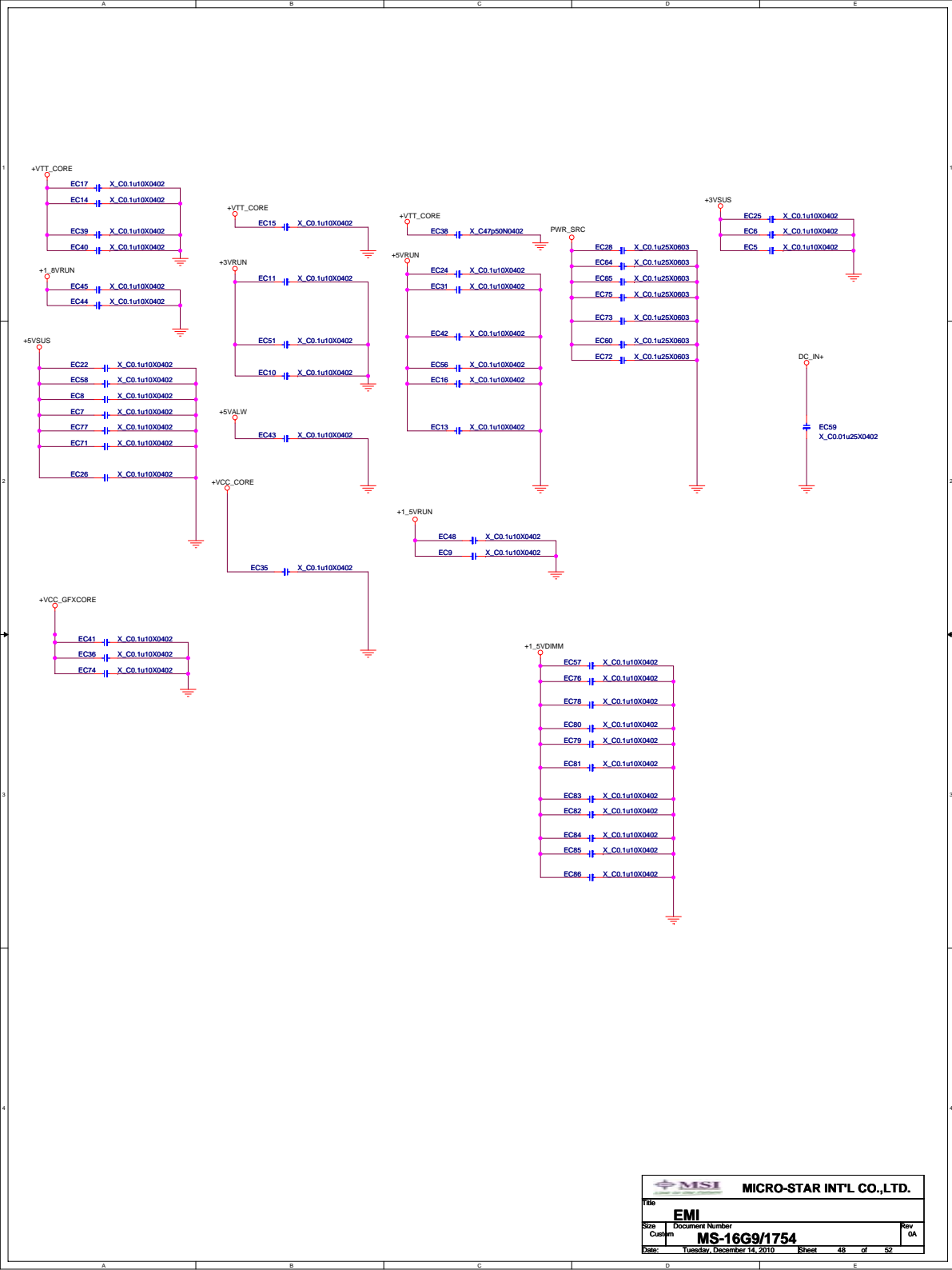
MSI Micro-Star International Co., Ltd.		
Title TP& LED		
Size B	Document Number MS-16G9/1754	Rev 0A
Date:	Sheet 46 of 52	



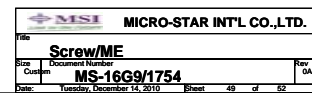
USB REVERSE

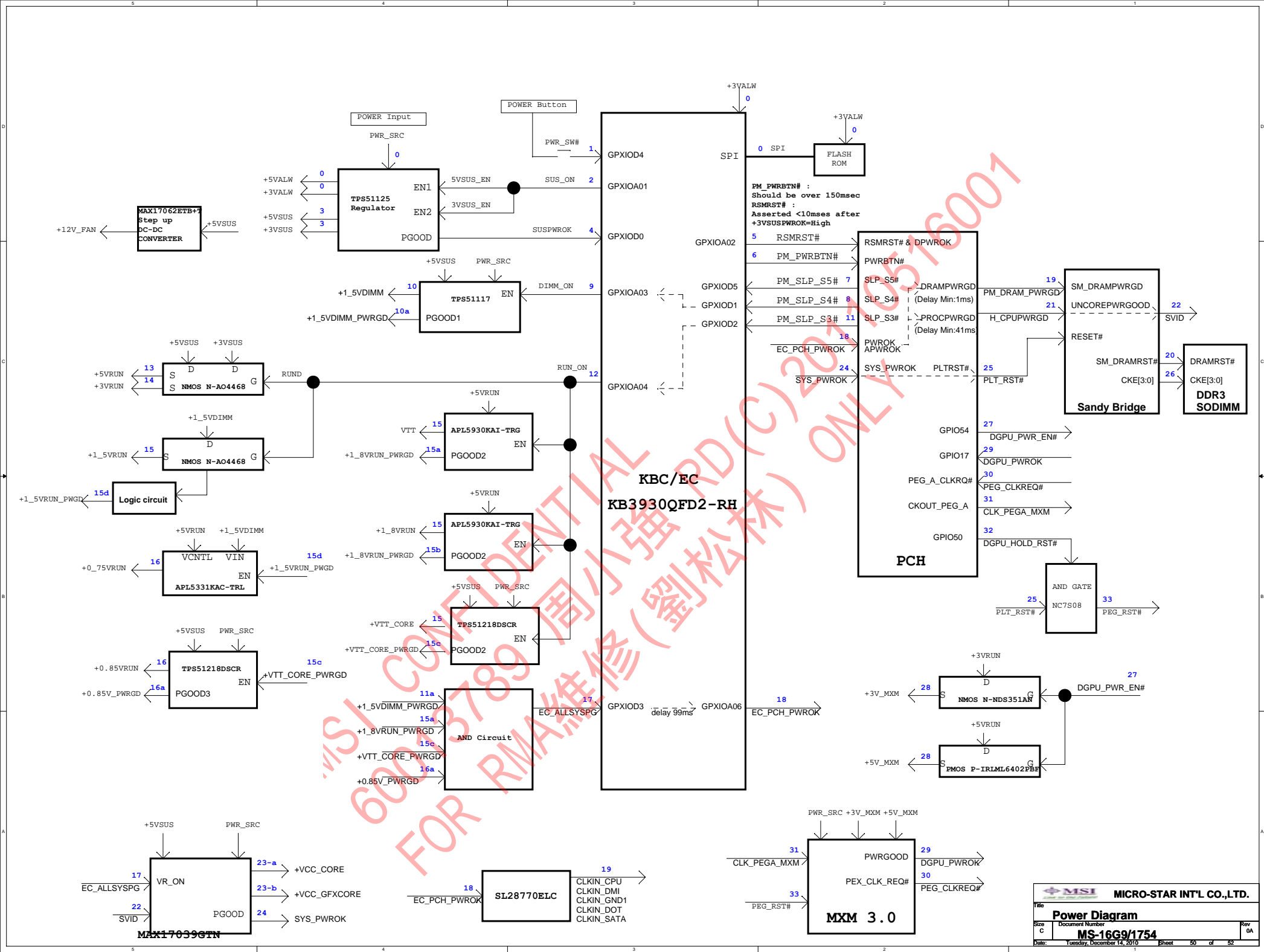


 <b>MICRO-STAR INT'L CO.,LTD.</b>	
Title	
<b>[E] USB2.0 PORT</b>	
Size B	Document Number
	<b>MS-1754</b>
Date:	Tuesday, December 14, 2010
Sheet	47 of 52
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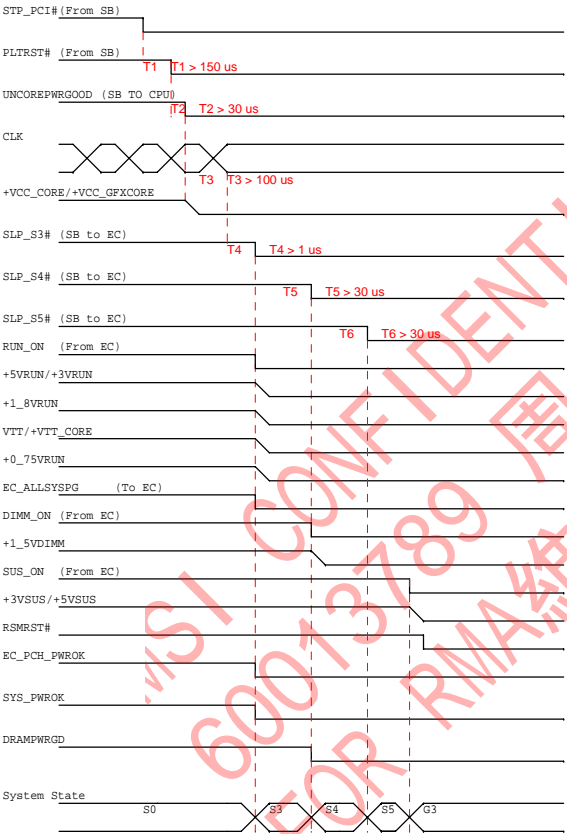




Power down Sequence DC mode S0 to G3

S0-S5

EC programming timing  
Intel Huron River timing SPEC



# S5-S0

EC programming timing

Intel Huron River timing SPEC

